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ARMY TM 11-5895-404-14-1
NAVY NAVELEX 0967-LP-301-5090
AIR FORCE TO 31S5-2FYA10-31-1

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OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL

SYSTEM STATUS AND CONTROL CONSOLE GROUP

OJ-50/FYA-10(V)

(NSN 7440-00-933-9077)

DEPARTMENTS OF THE ARMY, THE NAVY, AND THE AIR FORCE

7 FEBRUARY 1985

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WARNING

DANGEROUS CHEMICALS

Adequate ventilation should be provided while using TRICHLOROTRIFLUOROETHANE. Prolonged breathing of vapor should be avoided. The solvent should not be used near heat or open flame; the products of decomposition are toxic and irritating. Since TRICHLOROTRIFLUOROETHANE dissolves natural oils, prolonged contact with skin should be avoided. When necessary, use gloves which the solvent cannot penetrate. If the solvent is taken internally, consult a physician immediately.

DANGEROUS VOLTAGE

Make certain that all primary ac power is disconnected from the equipment and that all front panel power switches are turned off when removing or replacing power supplies.

HEAVY WEIGHT

The power supplies are extremely heavy. A minimum of two people should be used to remove a power supply from the cabinet.

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5 SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

1. DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL
2. IF POSSIBLE , TURN OFF THE ELECTRICAL POWER
3. IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL
4. SEND FOR HELP AS SOON AS POSSIBLE
5. AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

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Technical Manual
No. 11-5895-404-14-1
Technical Manual
NAVELEX 0967-LP-301-5090
Technical Order
No. 31S5-2FYA10-31-1

DEPARTMENTS OF THE ARMY,
THE NAVY, AND THE AIR FORCE

Washington, DC, *7 February 1985*

OPERATOR'S, ORGANIZATIONAL, DIRECT SUPPORT, AND GENERAL SUPPORT MAINTENANCE MANUAL

SYSTEM STATUS AND CONTROL CONSOLE GROUP

OJ-50/FYA-10 (V)

(NSN 7440-00-933-9077)

This volume contains chapters 1 through 5, appendixes A through D, and the index. The logic diagrams are contained in TM 11-5895-404-15-2/NAVELEX 0967-LP-301-5100/TO 31S5-2FYA10-31-2.

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward direct to prime ALC/MST.

For Navy, mail comments to the Commander, Naval Electronics Systems Command, ATTN: ELEX 8122, Washington, DC 20360.

In either case, a reply will be furnished direct to you.

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*This manual supersedes TM 11-5895-404-15/1/NAVSHIPS 0967-301-5090/TO 31S5-2FYA10-31, 14 October 1968, including all changes.

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CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual contains operation and maintenance information for Console Group, System Status and Control OJ-50/FYA-10(V) (fig. 1-1), hereinafter referred to as the system status and control console (SSCC). This manual contains five chapters described as follows: chapter 1 contains information regarding the purpose and capabilities of the SSCC, a brief discussion of the functional relationship of the SSCC to other units of the automatic digital message switching (ADMS) center, a list of the main technical characteristics of the SSCC, and a brief physical description; chapter 2 contains the installation procedures; chapter 3 contains information describing the purpose and location of the operator's controls and indicators; chapter 4 describes the functional operation of the SSCC; and chapter 5 contains information required for the preventive and corrective maintenance of the SSCC.

b. The complete series for the console consists of two manuals: TM 11-5895-404-14-1, as described in *a* above, and TM 11-5895-404-15/2, which consists of the logic diagrams.

c. Throughout this manual, where appropriate, references are made to other publications which contain information applicable to the operation and maintenance of the SSCC. A complete listing of applicable reference publications is provided in appen dix A.

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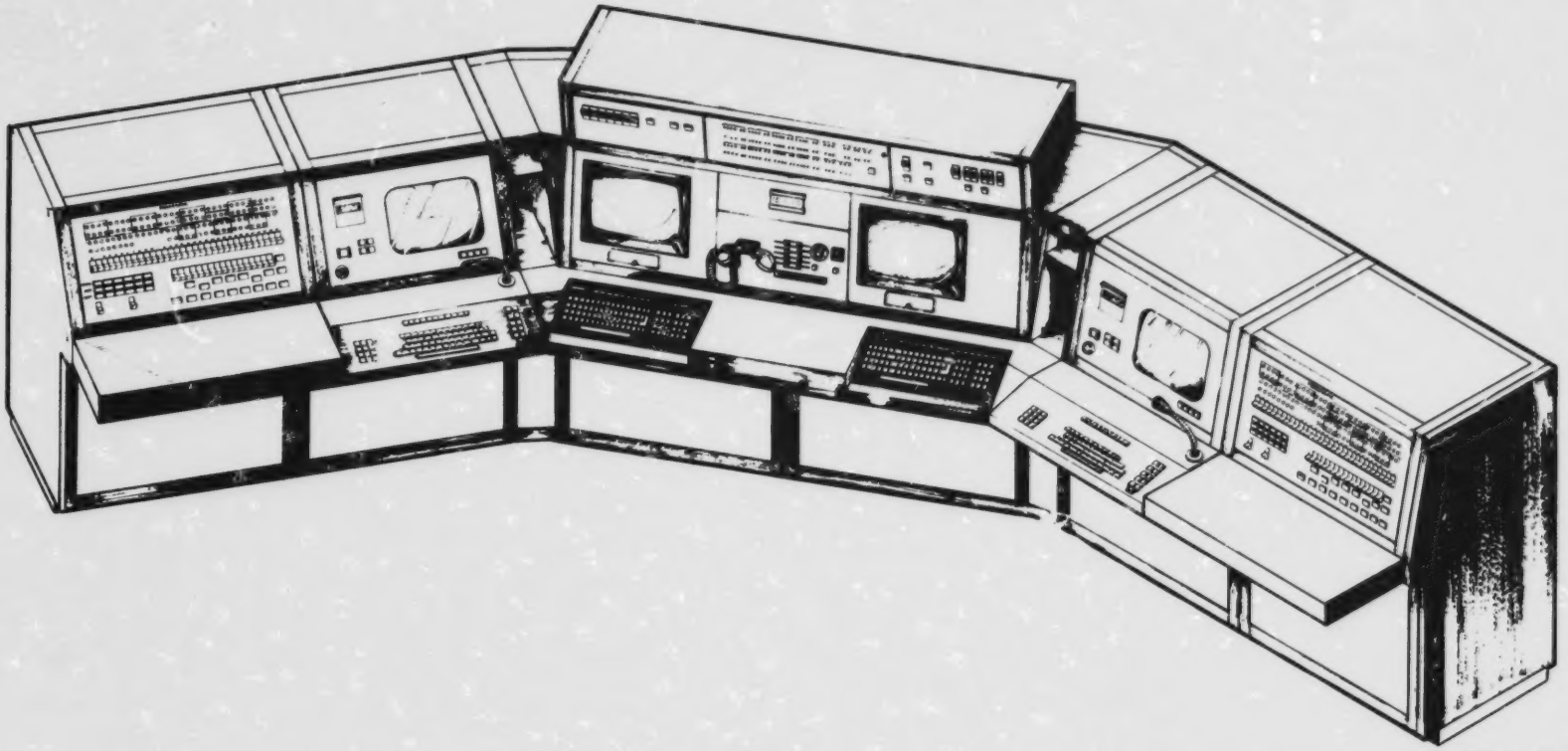

Figure 1-1. Console Group, System Status and Control OJ-50/FYA-10(V)

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d. The maintenance allocation chart (MAC) appears in appendix B, and the repair parts and special tools list (RPSTL) appears in TM 11-5895-404-40P.

1-2. Consolidated Index of Army Publications and Blank Forms

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to your equipment.

1-3. Maintenance Forms, Records, and Reports

a. Report of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by DA Pam 738-750, as contained in Maintenance Management Update. Air Force personnel will use AFR 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Subsystem (MDCS) IAW OPNAVINST 4790.2 Vol 3 and unsatisfactory material/conditions (UR submissions) IAW OPNAVINST 4790.2, Vol 2, chapter 17.

b. Report of Packaging and Handling Deficiencies. Fill out and forward 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73 AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AR 75-18/MCO P4610.19D/DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

a. Army. If your System Status and Control Console Group OJ-50/FYA-10(V) needs improvement, let us know. Send us and EIR. You, the user, are the only one who can tell us what you don't like about your equipment, Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. We'll send you a reply.

b. Air Force. Air Force personnel are encouraged to submit EIR's in accordance with AFR 900-4.

c. Navy. Navy personnel are encourage to submit EIR's through their local Beneficial Suggestion Program.

1-5. Administrative Storage

Administrative storage of equipment issued to and used by army activities shall be in accordance with TM 740-90-1.

1-6. Destruction of Army Electronics Materiel

Destruction of Army electronics material to prevent enemy use shall be in accordance with TM 750-244-2.

1-7. Purpose and Use

The SSCC provides operator interface to the six 102 processors, the bulk storage subsystem (BSS), the mass memories, and the LSI 11/2 microprocessors.

1-8. Description

a. General. The SSCC (fig. 1-2) consists of five sections (bays), A1 through A5. The assemblies contained in these sections are listed in table 1-1 and illustrated in figures 1-3 and 1-6. Leading particulars are listed in table 1-2.

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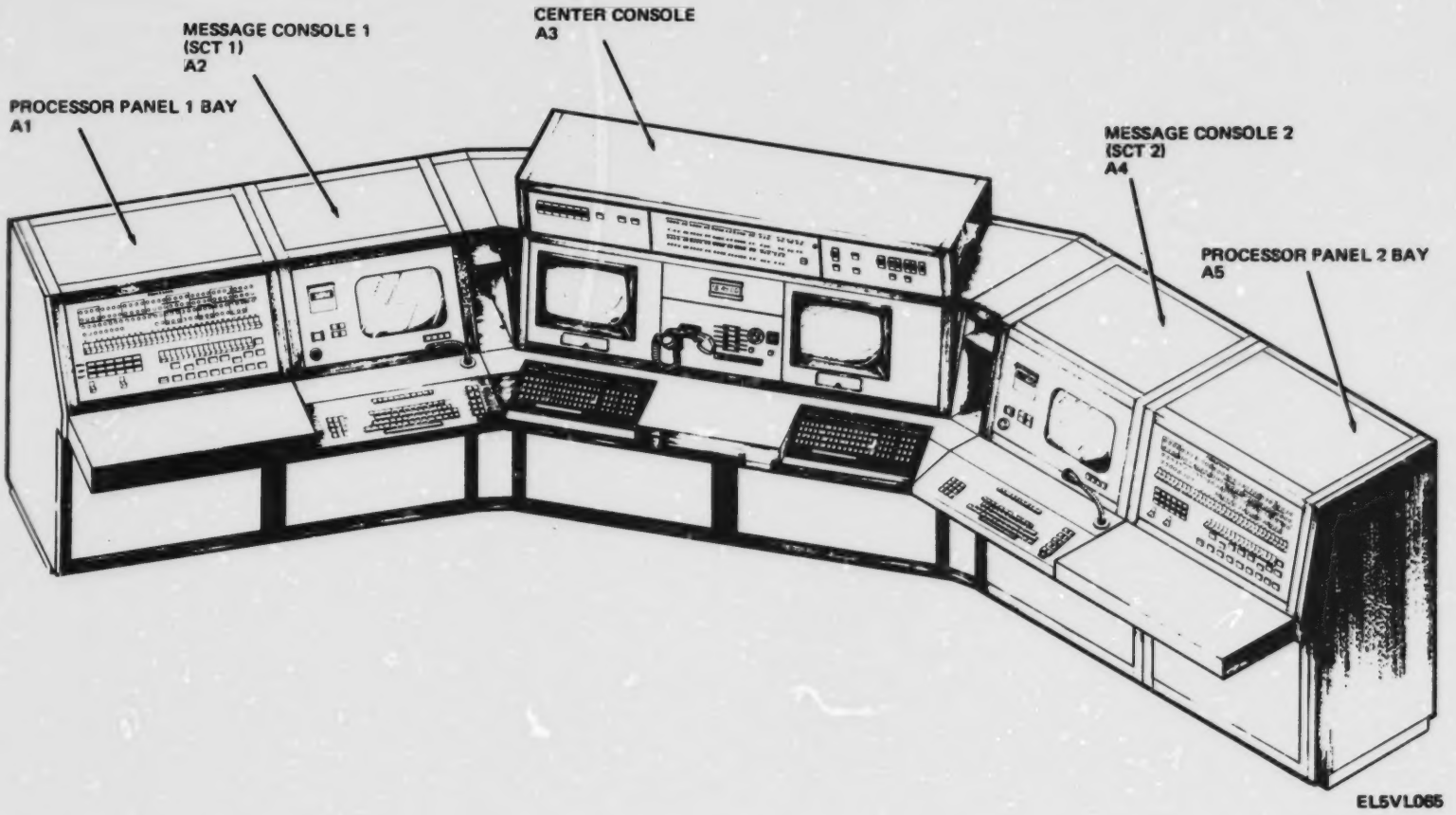

Figure 1-2. System Status and Control Console (SSCC), Front View.

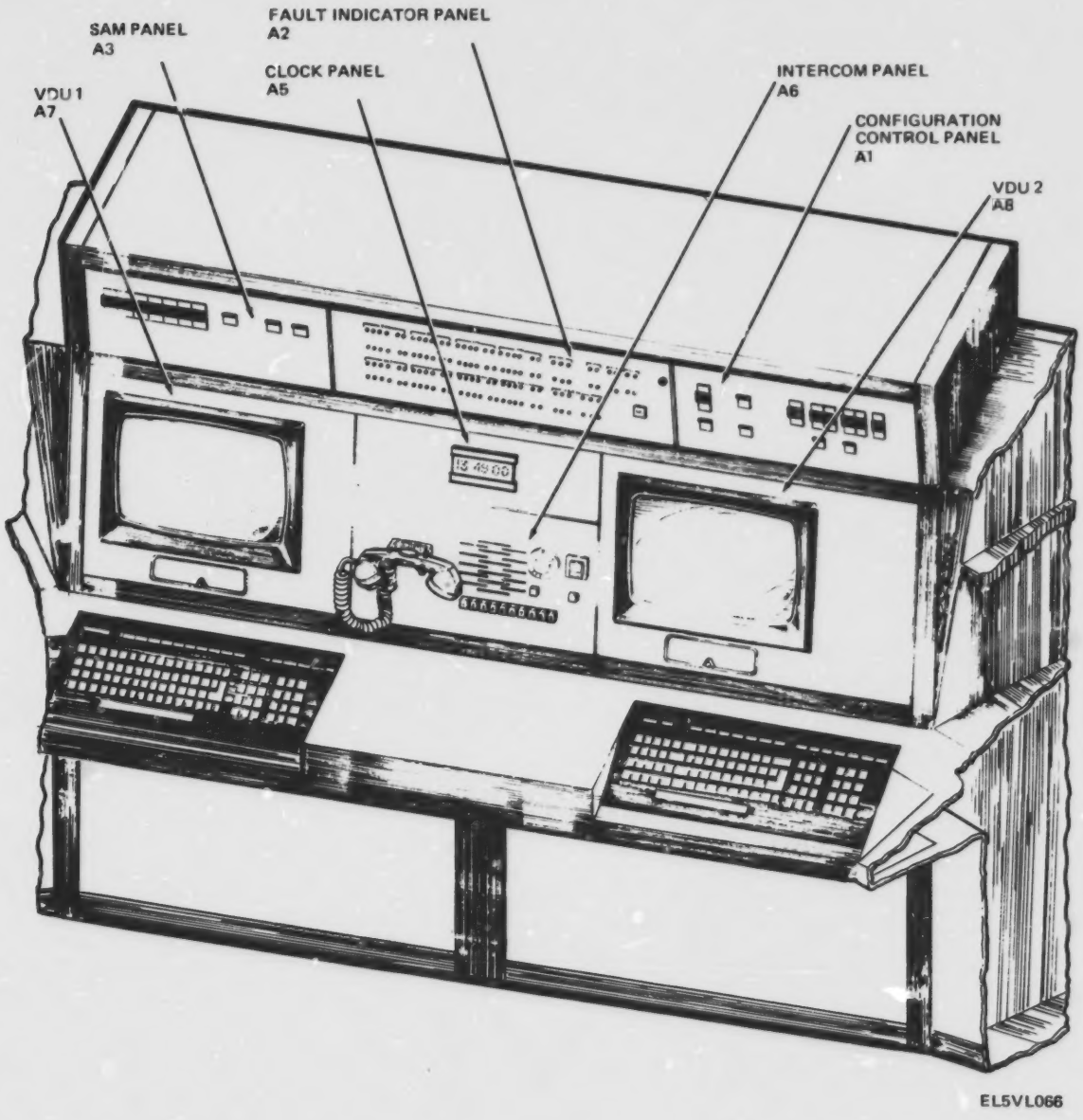

Figure 1-3. Center Console, A3, Front View.

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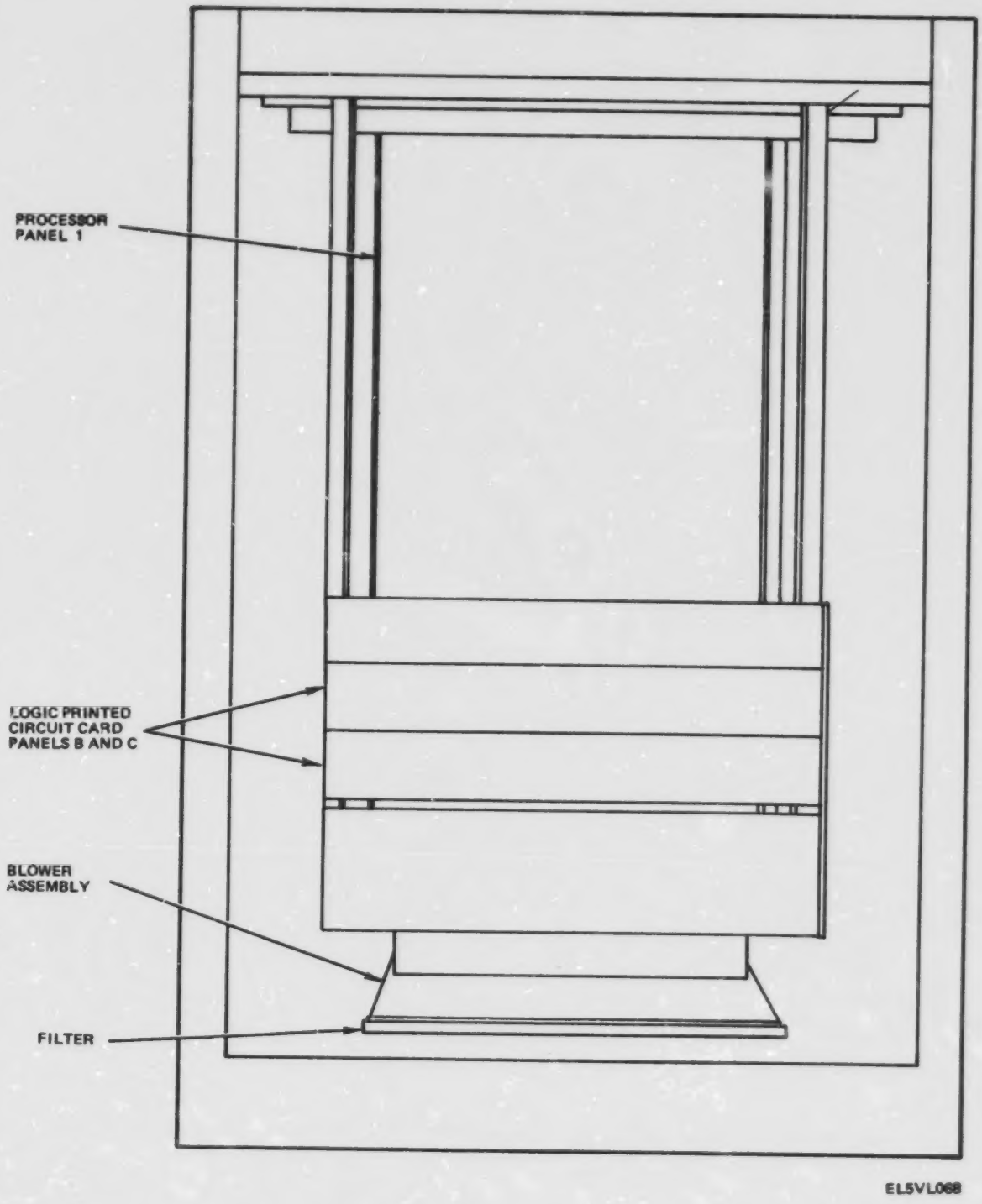

Figure 1-4. Processor Panel 1 Bay, A1, Rear View.

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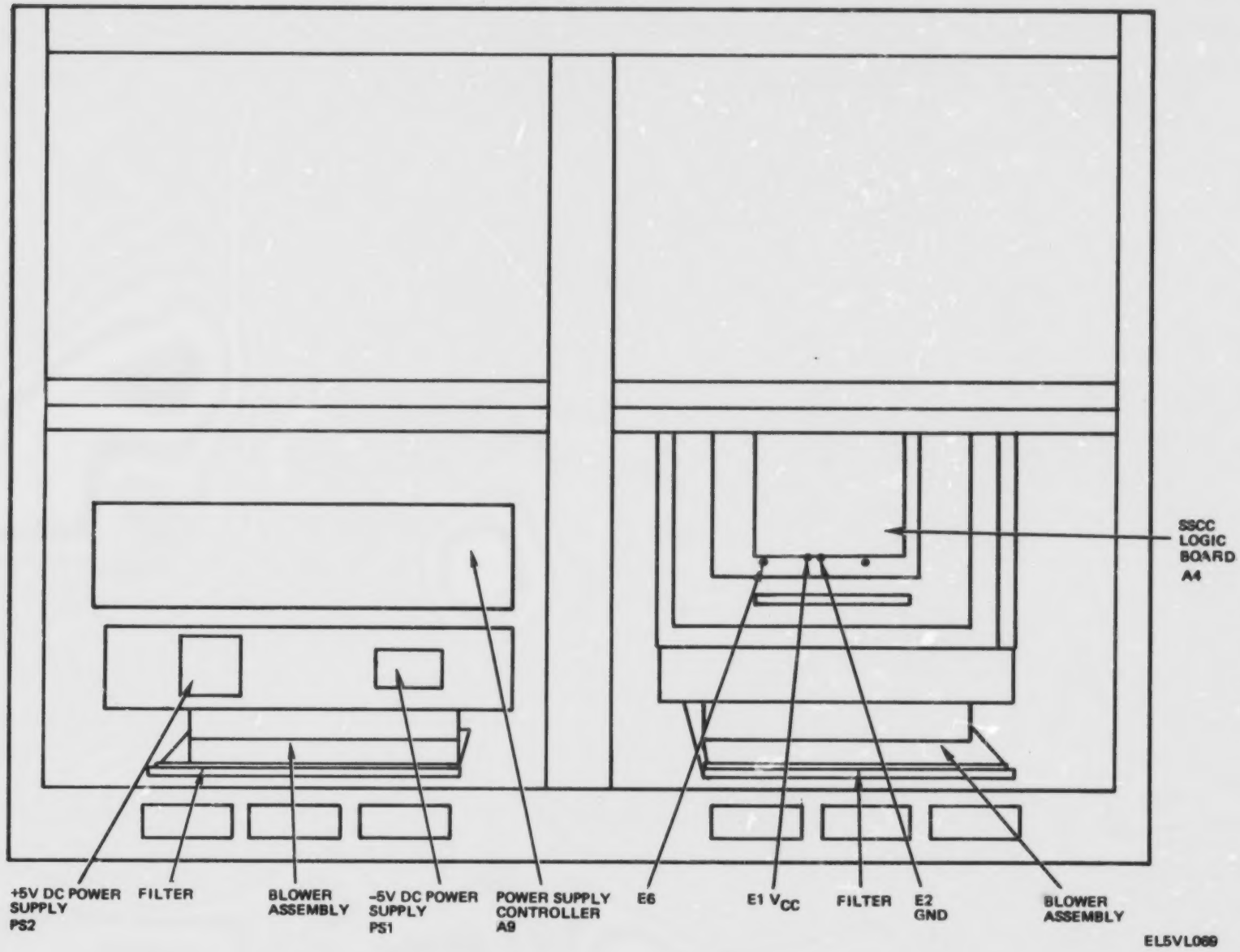

Figure 1-5. Center Console, A3, Rear View.

7.

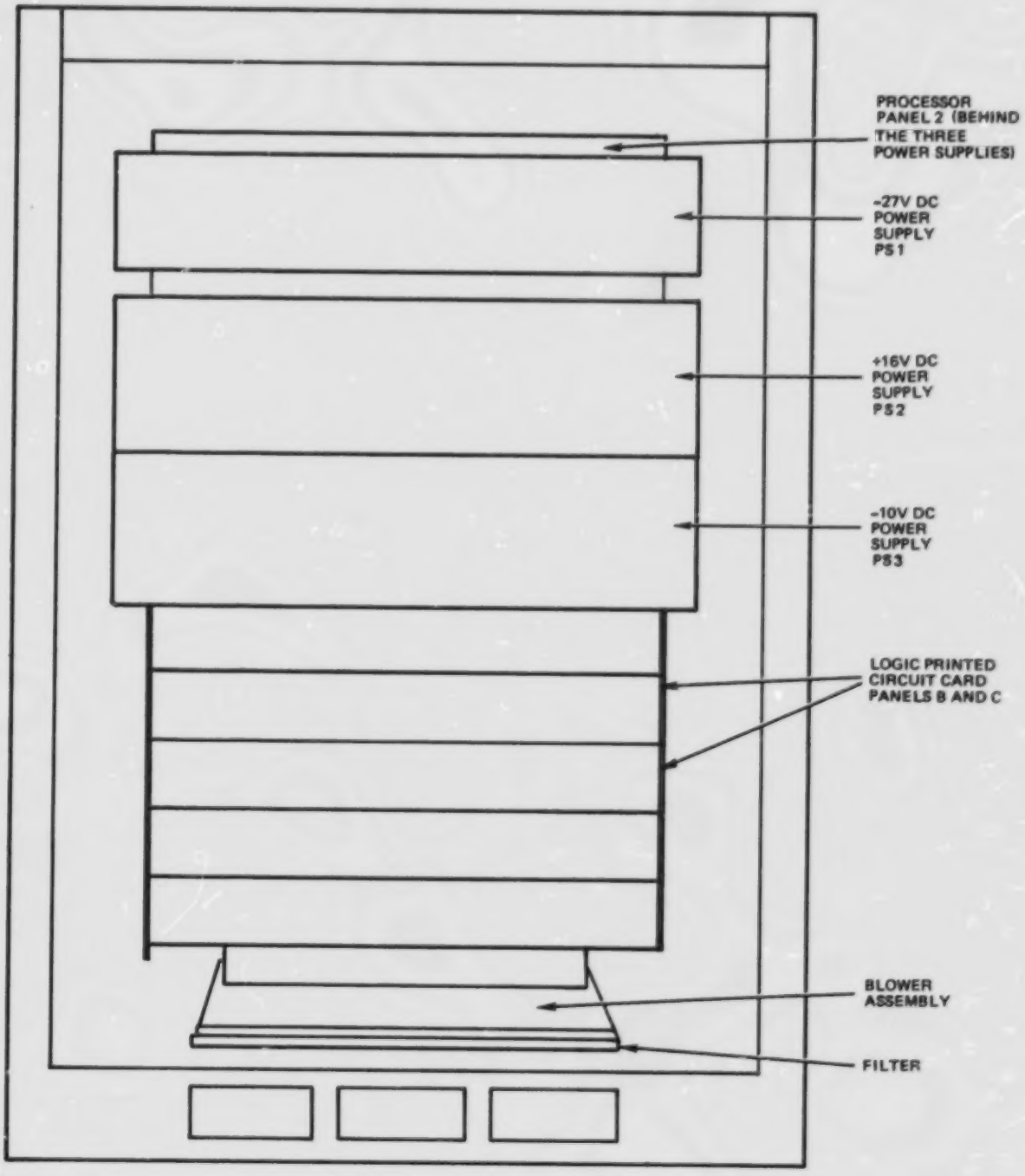
PROCESSOR PANEL 2 (BEHIND THE THREE POWER SUPPLIES)
-27V DC POWER SUPPLY PS1
+16V DC POWER SUPPLY PS2
-10V DC POWER SUPPLY PS3
LOGIC PRINTED CIRCUIT CARD PANELS B AND C
BLOWER ASSEMBLY
FILTER
EL5VL071

Figure 1-6. Processor Panel 2 Bay, A5, Rear View.

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Table 1-1. Equipment List

Ref des	Official nomenclature	Common name
	Console Group, System Status and Control OJ-50/FYA-10(V)	System status and control console (SSCC)
A1		Processor panel 1 bay
		Processor panel 1
A2	Console, Message OJ-347/FYA-10(V)	Message console 1 (also known as system command terminal (SCT) 1)
A3		Center console
A1		Configuration control panel
A2		Fault indicator panel
A3		System autoload module (SAM) panel
A4		SSCC logic board
A5		Clock panel
A6	Intercommunication Station LS-661/FYA	Intercom panel
A7	Digital Data Terminal AN/FYQ-89	Video display unit (VDU) 1
A8	Digital Date Terminal AN/FYQ-89	Video display unit (VDU) 2
A9	Power Supply Controller C-7225/FYA-10(V)	Power supply controller
PS1	Power Supply PP-7604/U	−5 V dc power supply
PS2	Power Supply PP-7603/U	+5 V dc power supply
A4	Console, Message OJ-347/FYA-10(V)	Message console 2 (also known as system command terminal (SCT) 2)
A5		Processor panel 2 bay
		Processor panel 2
PS1	Power Supply PP-4751/FYA-10(V)	−27 V dc power supply
PS2	Power Supply PP-4754/FYA-10(V)	+16 V dc power supply
PS3	Power Supply PP-4755/FYA-10(V)	−10 V dc power supply

Table 1-2. Leading Particulars

Section	Quantity	Height (in)	Depth (in)	Width (in)	Weight (lb)
A1	1	50	42	35	
A2	1	50	42	37	
A3	1	58	42	68	2600
A4	1	50	42	37	
A5	1	50	42	35	

b. Power Supplies. The SSCC contains five power supplies and a power supply controller. The +5 V dc and −5 V dc power supplies and the power supply controller are mounted in the rear of section A3. The −27 V dc, +16 V dc, and −10 V dc power supplies are mounted in the rear of section A5.

c. System Autoload Module (SAM) Panel. The system autoload module (SAM) panel contains touch-activated switches for selecting an operating configuration, a switch for starting a processor, and indicators for monitoring start, operate, and fault conditions. Logic circuits for SAM functions are located on the SSCC logic board.

d. Fault Indicator Panel. The fault indicator panel contains indicators for fault and status monitoring of the processor memories, mass memories, message consoles, and bulk storage subsystem. Power supply failure indicators display fault conditions of the configuration switch controller power supplies. Logic circuits for fault indicator panel functions are located on the SSCC logic board.

e. Configuration Control Panel. The configuration control panel provides touch-activated switches to select the operational configuration switch controller (CSC) and the monitor control. Status lights on the panel display monitor control status. Logic circuits for configuration control panel functions are located on the SSCC logic module board.

f. SSCC Logic Board. The SSCC logic board is mounted on an aluminum frame which is inside the center console.

g. Video Display Units. Two identical and interchangeable video display units (VDU's) and their associated keyboards provide channel status, subsystem status, and other requested parameter status. For a detailed description of the VDU, refer to TM 11-5895-1094-14.

h. Intercom Panel. The intercom panel includes a hand instrument and speaker system to permit listening and talking without lifting the handset. An audio level control is provided on the panel. For a

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detailed description of the unit, refer to TM 11-5895-416-15.

i. Message Consoles. Two message consoles permit operators to communicate with the associated computer to control and monitor the online automatic digital message switching center. Each message console includes a crt display, keyboard assembly, tape cassette, and a power supply assembly, mounted in a steel cabinet. For a detailed description of the message console, refer to TM 11-5895-839-14.

j. Processor Panels. The two processor panels interface with selected 102 processors through the configuration switch unit. Each panel has the controls and indicators necessary for manually loading or modifying the instructions and data for a processor under test. The panel also permits the operator to select continuous or single-step operating modes and to select certain processor register contents for display.

k. Clock Panel. The clock panel is mounted in the center of the SSCC. The display is in decimal 24-hour format consisting of hours, minutes, and seconds. The clock panel requires only ac input, and the only output is the visual display; it does not interface with the logic of the SSCC.

1-9. System Application

Either of two processor panels can be used to control any one of six 102 processors and to observe the contents of selected processor registers. The online 102 processor may be selected manually and started with controls on the system autoload module. The system autoload module also interfaces the message consoles, history packs, bulk storage subsystems, and configuration switch controller for selection of the online configuration. Two keyboards on the visual display units are used to request data from either LSI 11/2 microprocessor and display the requested data on the respective unit. The fault indicator panel monitors the bulk storage subsystem, mass memories, configuration switch controller, and 102 processor memories for fault and unit unavailable status. The fault indicator panel and processor panels also monitor and display status of the 102 processors for halt, parity, command fault, and step status.

1-10. Technical Characteristics

a. Environmental Conditions.

Ambient temperature	60 to 80° F (16 to 27° C)
Relative humidity	45% to 65%
Operating altitude	Sea level to 10,000 feet above sea level

b. Power Requirements.

Ac power	Two single-phase inputs at 120 ±5 V ac, 60 ± 3 Hz

c. Logic Levels.

Processor panel logic HIGH	0.0 +0.5 V dc
Processor panel logic LOW	−5.0 ± 0.5 V dc
SSCC logic HIGH	+2.4 to +5.0 V dc
SSCC logic LOW	0.0 to +0.6 V dc

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CHAPTER 2

INSTALLATION

2-1. Tools, Test Equipment, and Materials Required

For installation of the SSCC, use appropriate items listed in appendix C.

NOTE

SSCC electrical wiring and interface cabling may already be installed and connected to the OJ-50/FYA-10(V). If so, the following subparagraphs 2-2*a* through 2-2*c* do not apply.

2-2. Installation Procedures

a. Installation of Cabling. Figure 2-1 shows the SSCC termination point of the signal cables for the unit. It also indicates the terminating equipment for the remaining end of the cable. Proper cabling installation is easily determined by using the interface cabling chart in *b* below in conjunction with figure 2-1.

NOTE

Paddle-type connectors are identified on the board near the bracket end of the connector.

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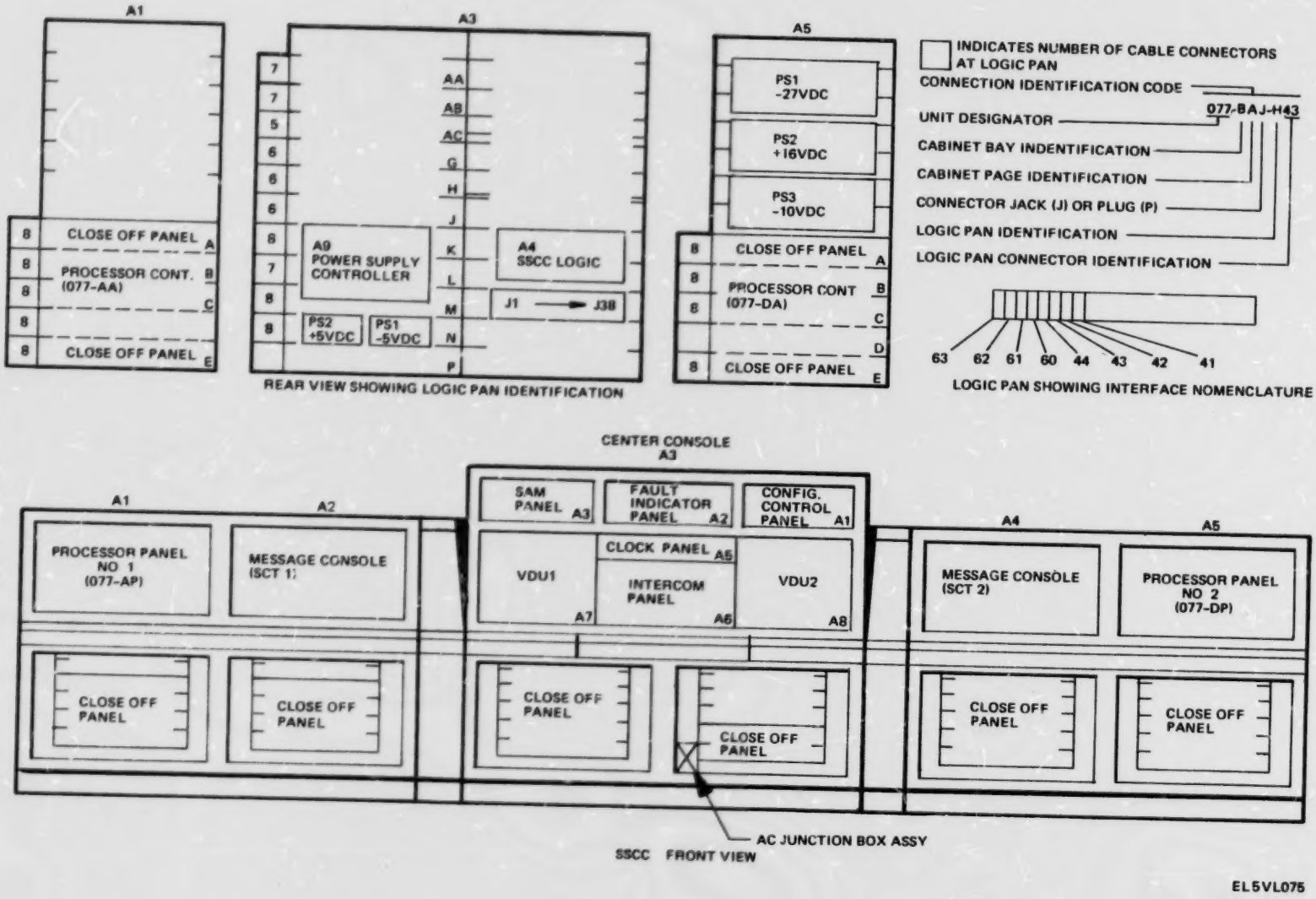

12.

Figure 2-1 ①. SSCC Cable Connector Location Diagram (Sheet 1 of 2).

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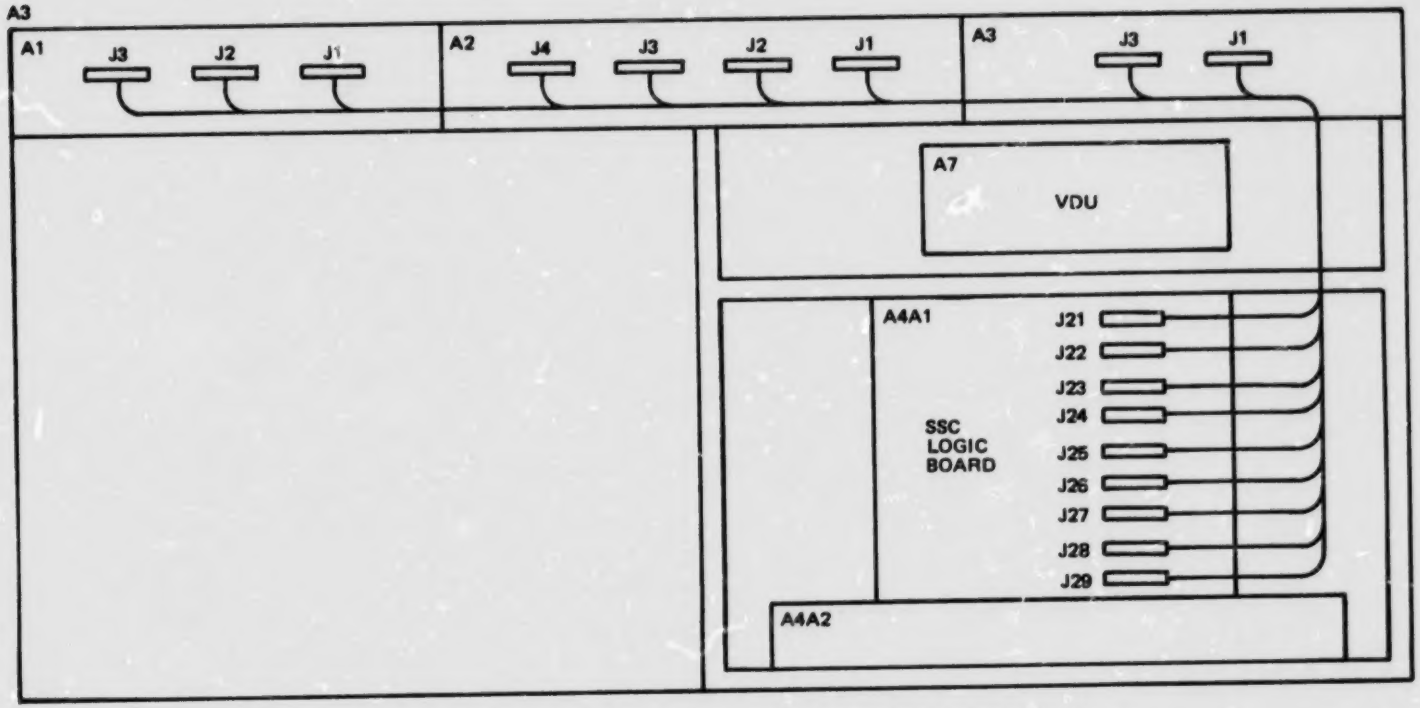

REAR VIEW SHOWING INTERNAL SIGNAL CABLE ROUTING (RIBBON CABLES)

CABLE PART NO	CABLE DESIGNATION	FROM	TO
284370-01	W1	A4A1 J21	A2J1
284370-02	W2	A4A1 J22	A2J2
284370-03	W3	A4A1 J23	A2J3
284370-04	W4	A4A1 J24	A2J4
284370-05	W5	A4A1 J25	A1J1
284370-06	W6	A4A1 J26	A1J2
284370-07	W7	A4A1 J27	A1J3
284370-08	W8	A4A1 J28	A3J1
284370-09	W9	A4A1 J29	A3J3

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Figure 2-1(2). SSCC Cable Connector Location Diagram (Sheet 2 of 2).

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b. SSCC Interface Cabling. The following list identifies the cables between the SSCC and other units of the system. For the majority of the cables, the identification code system is as described in figure 2-1. For other cables a code system based on the installation floor plan identification number (eg. 0803 is the SSCC) and reference designator is used.

From SSCC Interface	*To External Interface Equipment Identification*
0803-A4A2-J01	0301-CA03A5-XCJ31
0803-A4A2-J03	0302-CA03A5-XCJ31
0803-A4A3-J09	0305-CA03A5-XCJ31
0803-A4A2-J011	0306-CA03A5-XCJ31
0803-A4A2-J13	084-BDJ-F03 Config. Control & Sensing Unit
0803-A4A2-J15	OFJ/1-00J-E44
0803-A4A2-J17	OFJ/1-00J-B44
0803-A4A2-J19	OFJ/2-00J-E44
0803-A4A2-J21	OFJ/2-00J-B44
0803-A4A2-J23	OGU/1-00J-B43
0803-A4A2-J25	OGU/1-00J-A41
0803-A4A2-J27	OGU/2-00J-B43
0803-A4A2-J29	OGU/2-00J-A41
0803-A4A2-J33	096-AAJ-D44 MTSS Console
0803-A4A2-J31	6103-A3-J73 Bulk Storage Subsystem
0803-A4A2-J35	0351-A1
0803-A4A2-J37	0352-A1 PDP 11/34
0803-VDU1-J1	0361-A6-J4
0803-VDU2-J1	0361-A6-J5
Processor Panel No. 1 (Bay A)	Maintenance console and tape configuration switch
077-AAJ-B41	097-BFJ-K02
B42	K03
B43	K04
B44	J03
B60	J04
B61	K01
B62	L01
B63	L02
C41	L03
C44	J02
D41	H03
D43	F04
D61	J01
D62	H04
E41	H01
E43	F02
E60	F03
077-AAJ-E62	097-BFJ-H02
Processor Panel No. 2 (bay D)	Maintenance console and tape configuration switch
077-DAJ-B41	097-BJJ-D02
B42	D03
B43	D04
B44	C03
B60	C04
B61	D08
B62	E01
B63	E02
C41	E03
C44	C02
D41	B03
D43	A04
D61	C01
D62	B04
E41	B01
E43	A02
E60	A03
077-DAJ-E62	097-BJJ-B02
077-DAJ-C63	Configuration switch distribution unit 106-ALJ-A03

c. Supplementary Wiring Diagrams. AC controller wiring table 590-1151 in TM 11-5895-747-15/1 provides a tabulation of the primary ac power wiring. DC power distribution is shown in figure 4-12.

2-3. Initial Check and Adjustment of Equipment

After installing the SSCC in accordance with instructions in paragraph 2-2 and prior to placing the equipment in operation, the following initial checks and adjustments must be performed.

a. Visual Checks.

(1) Check to see that all connector paddles are securely connected to their mating receptacles.

(2) Check all module panels to ensure that each module is securely seated in its connector.

b. Electrical Checks and Adjustments. No adjustments, alinements, or calibrations (excluding power supply adjustments) are required for the SSCC. No adjustments are required for the single-shot multivibrator (SS) circuits employed in the SSCC. For power supply adjustments refer to table 5-2.

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CHAPTER 3

OPERATING INSTRUCTIONS

Section I. CONTROLS AND INDICATORS

3-1. General

This section provides information regarding the location and function of controls and indicators of the system status and control console (SSCC). For the remaining console equipment, refer to the applicable manual referenced in chapter 1.

3-2. Controls and Indicators

a. System Autoload Module (fig. 3-1).

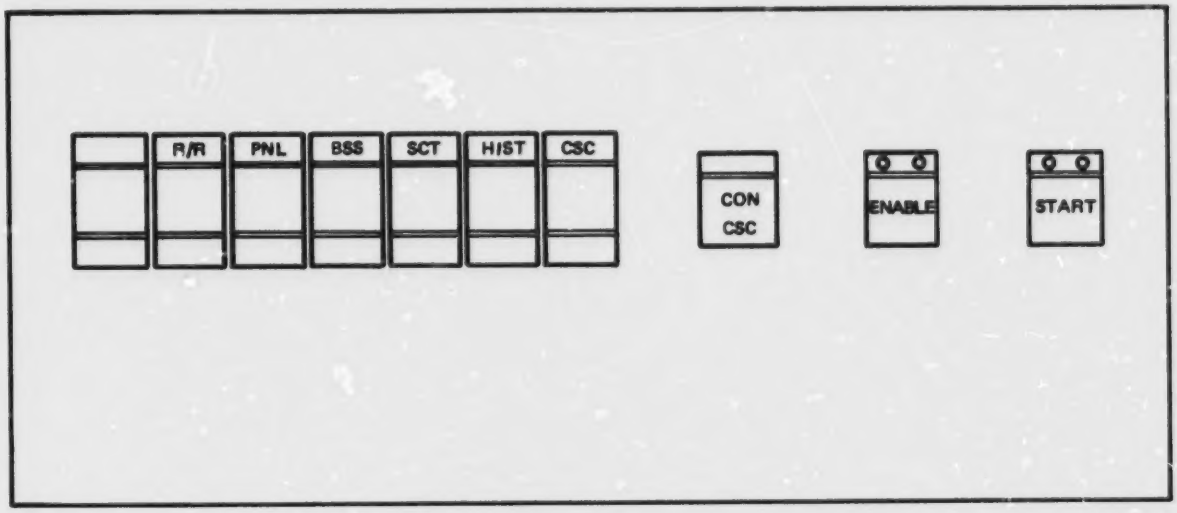

Figure 3-1. System Autoload Module Panel, Controls and Indicators.

Control or indicator	*Function*
R/R (touch-activated switch with numerical readout)	When *0* is displayed, reload and restart functions are disabled. When *1* is displayed, reload is enabled. When *2* is displayed, restart is enabled.
PNL (touch-activated switch with numerical readout)	When *0* is displayed, processor panel 1 is automatically selected. When *1* or *2* is displayed, the respective processor panel has been selected.
BSS (touch-activated switch with numerical readout)	When *0* is displayed, no bulk storage subsystem is selected. When *1* or *2* is displayed, the respective bulk storage subsystem has been selected.
SCT (touch-activated switch with numerical readout)	When *0* is displayed, no system command terminal is selected. When *1* or *2* is displayed, the respective system command terminal has been selected.
HIST (touch-activated switch with numerical readout)	When *0* is displayed, history balance is not to be performed. When *1* is displayed, history balance is to be performed.
CSC (touch-activated switch with numerical readout)	When *0* is displayed, no configuration switch controller (CSC) is selected. When *1* or *2* is displayed, the respective configuration switch controller is selected. The manual CON CSC switch will connect the CSC. Otherwise, ENABLE and START switches must be touched once function is selected.
CON CSC (touch-activated switch)	Switch activation causes a manual connection of the configuration switch controller selected by CSC switch. If CSC switch displays *0*, no CSC is selected. Touching CON CSC will dis-

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Control or indicator	*Function*
	able all other panel switches during manual connection.
ENABLE (touch-activated switch with two yellow lamps)	Switch activation will enable the system autoload module. This is indicated by both yellow lamps flashing. Touching START switch will begin autoload and extinguish yellow lamps. A second activation of the ENABLE switch will disable autoload.
START (touch-activated switch with one green and one read lamp)	Switch activation will initiate autoload sequence. Green lamp will illuminate to indicate a normal startup with processor running. Green lamp will extinguish when startup is complete. Red lamp will illuminate to indicate a fault condition and the processor has stopped.

b. Fault Indicator Panel (fig. FO-2).

Control or indicator	*Function*
PROC 1 FAULT M1 through M4 indicator lamps (red) (M5 not used)	Illuminates to indicate a fault condition is in effect for a memory unit in processor 1.
PROC 1 FAULT C indicator lamp (red)	Illuminates to indicate a command fault has been detected in processor 1.
PROC 1 FAULT P indicator lamp (red)	Illuminates to indicate a parity error has been detected in processor 1.
PROC 1 U/U M1 through M4 indicator lamps (amber) (M5 not used)	Illuminates to indicate a memory unit is unavailable and on line in processor 1.
PROC 1 U/U S indicator lamp (amber)	Illuminates to indicate processor 1 has stopped.
PROC 1 U/U H indicator lamp (amber)	Illuminates to indicate processor 1 is in the halt condition.
PROC 2 FAULT M1 through M4 indicator lamps (red) (M5 not used)	Illuminates to indicate a fault condition is in effect for a memory unit in processor 2.
PROC 2 FAULT C indicator lamp (red)	Illuminates to indicate a command fault has been detected in processor 2.
PROC 2 FAULT P indicator lamp (red)	Illuminates to indicate a parity error has been detected in processor 2.
PROC 2 U/U M1 through M4 indicator lamps (amber) (M5 not used)	Illuminates to indicate a memory unit is unavailable and on line in processor 2.
PROC 2 U/U S indicator lamp (amber)	Illuminates to indicate processor 2 has stopped.
PROC 2 U/U H indicator lamp (amber)	Illuminates to indicate processor 2 is in the halt condition.
PROC 3 FAULT M1 through M4 indicator lamps (red) (M5 not used)	Illuminates to indicate a fault condition is in effect for a memory unit in processor 3.
PROC 3 FAULT C indicator lamp (red)	Illuminates to indicate a command fault has been detected in processor 3.
PROC 3 FAULT P indicator lamp (red)	Illuminates to indicate a parity fault has been detected in processor 3.
PROC 3 U/U M1 through M4 indicator lamps (amber) (M5 not used)	Illuminates to indicate a memory unit is unavilable and on line in processor 3.
PROC 3 U/U S indicator lamp (amber)	Illuminates to indicate processor 3 has stopped.
PROC 3 U/U H indicator lamp (amber)	Illuminates to indicate processor 3 is in the halt condition.
MMSS FAULT 1, 2, and 3 indicator lamps (red)	Illuminates to indicate a fault condition in mass memory subsystem 1, 2, or 3.
MMSS U/U 1, 2, and 3 indicator lamps (amber)	Illuminates to indicate mass memory subsystem 1, 2, or 3 is unavailable.
BSS FAULT 1 and 2 indicator lamps (green)	Indicator for the online BSS is illuminated and indicator for the offline BSS is extinguished.
BSS U/U 1 and 2 indicator lamps (amber)	Illuminates to indicate activity on the BSS to MCC bus.
CSC FAULT 1 and 2 indicator lamps (red)	Illuminates to indicate a fault condition in CSC 1 or 2.
CSC U/U 1 and 2 indicator lamps (amber)	Illuminates to indicate configuration switch controller 1 or 2 is unavailable.
P/S 1 10/16 indicator lamp (red)	Flashes to indicate either −10 V dc or +16 V dc power supply 1 in CCSU is down.
P/S 1 48 indicator lamp (red)	Flashes to indicate +48 V dc power supply 1 in CCSU is down.
P/S 2 10/16 indicator lamp (red)	Flashes to indicate either −10 V dc or +16 V dc power supply 2 in CCSU is down.
P/S 2 48 indicator lamp (red)	Flashes to indicate +48 V dc power supply 2 in CCSU is down.
PROC 4 FAULT M1 through M4 indicator lamps (red) (M5 not used)	Illuminates to indicate a fault condition is in effect for a memory unit in processor 4.
PROC 4 FAULT C indicator lamp (red)	Illuminates to indicate a command fault has been detected in processor 4.
PROC 4 FAULT P indicator lamp (red)	Illuminates to indicate a parity fault has been detected in processor 4.
PROC 4 U/U M1 through M4 indicator lamps (amber) (M5 not used)	Illuminates to indicate a memory unit is unavailable and on line in processor 4.
PROC 4 U/U S indicator lamp (amber)	Illuminates to indicate processor 4 has stopped.
PROC 4 U/U H indicator lamp (amber)	Illuminates to indicate processor 4 is in the halt condition.
PROC 5 FAULT M1 through M4 indicator lamps (red) (M5 not used)	Illuminates to indicate a fault condition is in effect for a memory unit in processor 5.
PROC 5 FAULT C indicator lamp (red)	Illuminates to indicate a command fault has been detected in processor 5.
PROC 5 FAULT P indicator lamp (red)	Illuminates to indicate a parity fault has been detected in processor 5.
PROC 5 U/U M1 through M4 indicator lamps (amber) (M5 not used)	Illuminates to indicate a memory unit is unavailable and on line in processor 5.
PROC 5 U/U S indicator lamp (amber)	Illuminates to indicate processor 5 has stopped.

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Control or indicator	*Function*
PROC 5 U/U H indicator lamp (amber)	Illuminates to indicate processor 5 is in the halt condition.
PROC 6 FAULT M1 through M4 indicator lamps (red) (M5 not used)	Illuminates to indicate a fault condition is in effect for a memory unit in processor 6.
PROC 6 FAULT C indicator lamp (red)	Illuminates to indicate a command fault has been detected in processor 6.
PROC 6 FAULT P indicator lamp (red)	Illuminates to indicate a parity fault has been detected in processor 6.
PROC 6 U/U M1 through M4 indicator lamps (amber) (M5 not used)	Illuminates to indicate a memory unit is unavailable and on line in processor 6.
PROC 6 U/U S indicator lamp (amber)	Illuminates to indicate processor 6 has stopped.
PROC 6 U/U H indicator lamp (amber)	Illuminates to indicate processor 6 is in the halt condition.
MAJOR ALARMS BATTERY DIS indicator lamp (amber)	Illuminates (after 5 minutes) to indicate system is on battery (discharge).
MAJOR ALARMS BATTERY 10M indicator lamp (red)	Illuminates (after 10 minutes) to indicate system has been on battery for 10 minutes.
MAJOR ALARMS BATTERY CYD indicator lamp (red)	Illuminates (after 15 minutes) to indicate battery is approaching limit and operator MUST begin to cycle down system.
MAJOR ALARMS STATIC UPS OL indicator lamp (green)	Illuminates to indicate solid state uninterrupted power supply is on line.
MAJOR ALARMS STATIC UPS SB indicator lamp (amber)	Illuminates to indicate solid state uninterrupted power supply is on standby.
MAJOR ALARMS STATIC UPS OFF indicator lamp (red)	Illuminates to indicate solid state uninterrupted power supply is manually switched off.
MAJOR ALARMS AC indicator lamp (red)	Illuminates to indicate primary (commercial) ac power has failed.
MAJOR ALARMS UPS indicator lamp (red)	Illuminates to indicate rotary uninterrupted power supply has failed.
MAJOR ALARMS EMR indicator lamp (red)	Illuminates to indicate system is running on backup generator.
MAJOR ALARMS BCL indicator lamp (red)	Illuminates to indicate system black clock has failed.
MAJOR ALARMS RCL indicator lamp (red)	Illuminates to indicate system red clock has failed.
MAJOR ALARMS ENV indicator lamp (red)	Illuminates to indicate the environment is out of tolerance. This can be caused by excessive temperatures or humidity.
ERROR RESET (touch-activated switch	Switch activation will clear all memory fault indicators and preclear system autoload module logic. Fault indicators latch when illuminated and must be reset manually.

c. Configuration Control Panel (fig. 3-2).

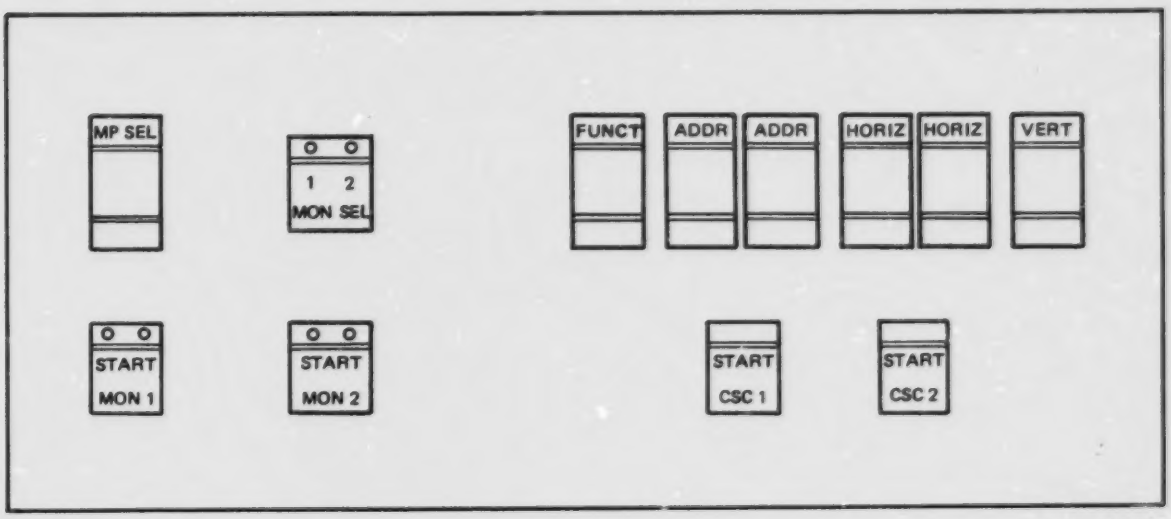

Figure 3-2. Configuration Control Panel, Controls and Indicators.

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Control or indicator	*Function*
MP SEL (touch-activated switch with numerical readout)	When *0* is displayed, no message processor is selected. When *1* through *6* is displayed, the respective message processor is selected.
MON SEL 1 or 2 (touch-activated switch with two yellow lamps)	Switch activation will select either monitor 1 or 2 and illuminate the yellow lamp above the selected number. Touching the switch again will select the opposite monitor.
START MON 1 (touch-activated switch with one yellow and one red lamp)	Switch activation will start monitor 1. Yellow lamp will illuminate to indicate monitor 1 is in standby. Red lamp will illuminate to indicate monitor 1 has timed out.
START MON 2 (touch-activated switch with one yellow and one red lamp)	Switch activation will start monitor 2. Yellow lamp will illuminate to indicate monitor 2 is in standby. Red lamp will illuminate to indicate monitor 2 has timed out.
START CSC 1 (touch-activated switch)	Switch activation will start configuration switch controller 1 for manual reconfiguration.
START CSC 2 (touch-activated switch)	Switch activation will start configuration switch controller 2 for manual reconfiguration.
FUNCT (touch-activated switch with numerical readout)	When *0* is displayed, no function is selected. Functions 1, 3, 4, 5, 8, and 9 are inactive. When *2* is displayed, mass memories (1-3) are connected to 102 processors (1-6). When *6* is displayed, processor panels (1-2) are connected to 102 processors (1-6). When *7* is displayed, communications lines/peripheral devices (1-16, 19, 21, and 22) are connected to 102 processors (1-6). On function *7*, configuration switch controller (CSC) for test (device 22), system command terminals (devices 19 and 21), and line termination buffers (devices 1 through 16) are all active.
ADDR (two touch-activated switches with numerical readouts)	When the combined switches display *00*, no address is selected. Otherwise, switches will select addresses *01* through *17* and reset to *00*.
HORIZ (two touch-activated switches with numerical readouts)	When the combined switches display *00*, no horizontal address code is selected. Otherwise, switches will select codes *01* through *17* and reset to *00*.
VERT (touch-activated switch with numerical readout)	Switch activation will select and display vertical address codes *0* through *4* and reset to *0*.

d. VDU (fig. 3-3, 3-4).

Control or indicator	*Function*
VDU Display	
POWER Switch	Controls 120 V ac input to video display unit.
BRIGHTNESS Potentiometer	Controls intensity of white characters on crt.
CONTRAST Potentiometer	Controls relative brightness between displayed characters and background.
VOLUME Potentiometer	Controls loudness of audio keyboard response and alarm.
VDU Keyboard	
ALL CAPS Key and Indicator	Engaging this key lights its LED indicator and shifts all alpha-symbol keys to the indicated upper case.
RESET Key	Not used.
BACK TAB Key	Used alone to move cursor back to last tab column. Used with SHIFT key to clear tab at present cursor position.
TAB Key	Used alone to move cursor to next tab setting. Used with SHIFT key to set tab at present cursor position.
Function Keys	Sixteen keys marked F1 through F16 (refer to table 3-14.1).
PAGE ↓ Key	Used to move display down by one data page (24 lines).*
PAGE ↑ Key	Used to move display up by one data page (24 lines).*
MODE Key	Used with TEST key on keyboard to enter self-test mode. Pressing any other alpha key ends the self test.
SCROLL ↑ Key	Used to move display up by one line.*
SCROLL ↓ Key	Used to move display down by one line.*
Decimal Key Pad	Ten digit keys plus a decimal-point key. Used to enter numeric command information.
Cursor Control Keys	Used to move cursor one line or one space in the direction indicated, or to the home position in the extreme upper left.
Typewriter Keyboard With Shift LOCK Indicator	Standard 96-key typewriter keyboard with LED indicator that lights to indicate shift LOCK engaged. Used for text and command entries.
CTRL Key	(To be determined)
ESG Key	Sends escape sequence.
PRINT DATA Key	(Not used)
PRINT SCAN Key	(Not used)

***PAGE and SCROLL operate within the limits of the beginning and the end of memory. If the operator attempts to PAGE or SCROLL beyond the limits of memory, the key stroke is ignored and characters are not lost. During a PAGE or SCROLL operation, the cursor remains in the same position relative to the screen. Operates only when in text editor mode.**

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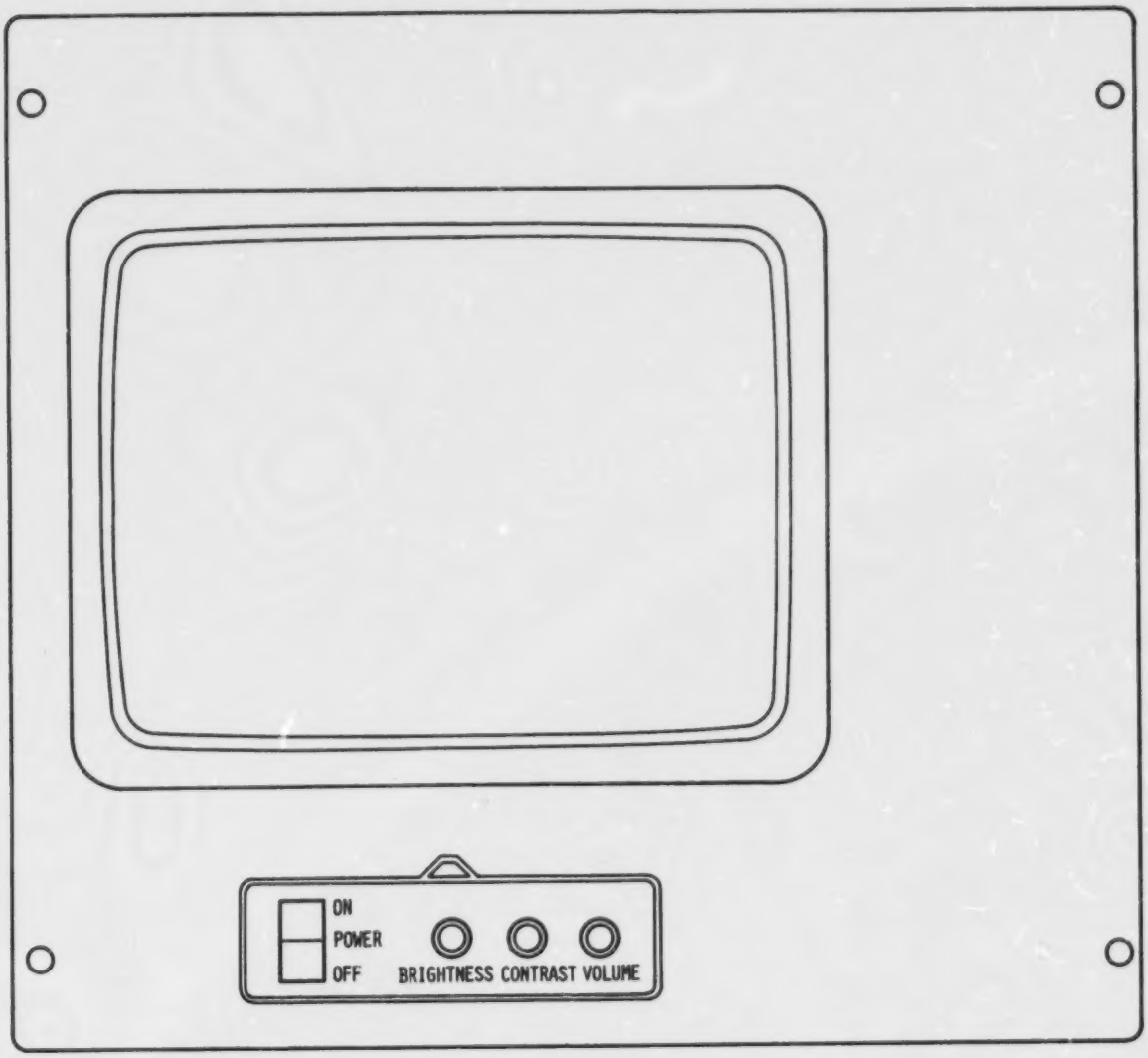

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Figure 3-3. VDU Control Panel, Controls and Indicators.

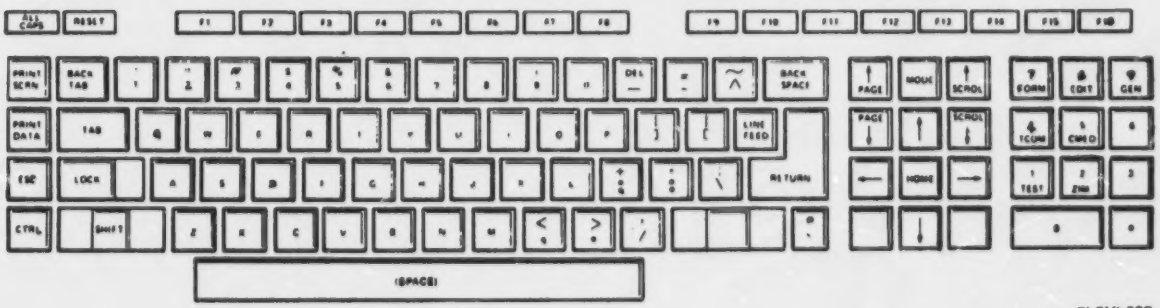

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Figure 3-4. VDU Keyboard, Controls and Indicators.

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e. Processor Unit to Panel Interface (fig. FO-3).

NOTE

Processor panel 2 is identical to processor panel 1.

Control or indicator	*Function*
R 0 through 31 indicator lamps (white)	Display current contents of R register. An illuminated indicator represents a "1" in respective bit position of R register.
D 0 through 31 indicator lamps (white)	Display current contents of D/I register. An illuminated indicator represents a "1" in respective bit position of D/I register.
INSTRUCTION REGISTER I through M indicator lamps (I-yellow, C_3-C_0-white, R_2-R_0-yellow, K-white, X_2-X_0-yellow, M-yellow)	Display current contents of instruction register. An illuminated indicator represents a "1" in respective bit position of instruction register.
OPERAND ADDRESS V_{16} through K_0 indicator lamps (V_{16}-V_0-white, K_0 and K_1-yellow)	Display current contents of operand address register. An illuminated indicator represents a "1" in respective bit position of operand address register.
PA V_{16} V_0 indicator lamps (white)	Display current contents of program address (PA) register. An illuminated indicator represents a "1" in respective bit position of PA register.
PROC indicator lamp (white)	Displays assignment status of common data section. When illuminated, common data section is assigned to processing assembly. When not illuminated, common data section is assigned to input/output control (IOC) section.
ADS indicator lamp (yellow)	Illuminates to indicate that processing assembly or IOC has been stopped because of an address comparison.
OVF indicator lamp (yellow)	Illuminates to indicate an overflow condition.
RUN indicator lamp (green)	Illuminates to indicate that either the processing assembly or IOC is functioning.
HALT indicator lamp (red)	Illuminates when processing assembly has executed a halt instruction.
CMDF indicator lamp (red)	Illuminates when a command fault (illegal instruction) has been encountered by processing assembly.
PARITY indicator lamp (red)	Illuminates to indicate detection of a parity error on a read from memory.
OAR V_{17} (blue)	Not used.

f. Processor Panel to Processor Unit Interface (fig. FO-3).

Control or indicator	*Function*
T (I through K_0), (32 two-position keyboard rocker switches, alternate black and white, in groups of four)	Sets up data that can be sampled by an instruction and transferred to memory as a processor function. T (V_{16} through V_0) rocker switch color groupings distinguish hexadecimal from octal coding. Yellow stripes are inscribed on rocker switches to distinguish octal coding.
KA (V_{16} through V_0), (17 two-position keyboard rocker switches, alternate black and white, in groups of three)	Sets up data that serves as address for memory stop, store, set scanner, load PA, and display functions. Color groupings identify octal coding.
OPERATE (IOC-BOTH-PROC, three-position rocker-type switch)	When switch is in IOC position, enables IOC to operate and inhibits processing assembly; BOTH position enables both the processing assembly and IOC to operate; PROC position enables processing assembly to operate and inhibits IOC.
FAULT ACTION (OVRD-INTER-STOP, three position rocker-type switch)	When switch is on OVRD (override) position, causes parity errors to be disregarded and a stop to occur on command faults; INTER (interrupt) position causes an interrupt to occur for either command or parity faults; STOP position causes processing assembly or IOC to stop on either command or parity faults.
TGL AS INST (alternate-action pushbutton-type switch/indicator (white))	Switch activation causes T keyboard (32-bit console register) to become instruction-accessed by processing assembly; when switch is activated, indicator illuminates.
TGL AS ACW (alternate-action push-button-type switch/indicator (white))	Switch activation causes T keyboard (32-bit console register) to become data to be moved by an IOMTA instruction encountered in the IOC list; when switch is activated, indicator illuminates.
IOC STOP (alternate-action pushbutton-type switch/indicator (white))	Switch activation causes IOC to stop if KA equals IOC memory address specified on a store or fetch; when switch is activated, indicator illuminates.
PROC STOP (alternate-action pushbutton-type switch/indicator (white))	Switch activation causes processing assembly to stop if KA equals processing assembly memory address specified on a store or fetch; when switch is activated, indicator illuminates.
SET SCANNER (momentary-contact pushbutton switch)	In step mode only, switch activation causes input/output scanner of character interface assembly (CIA) to become channel address value contained in KA.
RETAIN INST (alternate-action pushbutton-type switch/indicator (white))	Switch activation inhibits counting of PA register during processing assembly instructions and inhibits counting of sequence control word (SCW)

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Control or indicator	*Function*
	VW field during IOC instructions; when switch is activated, indicator illuminates.
SCANNER LOCK (alternate-action pushbutton-type switch/indicator (white))	Switch activation causes input/output scanner to remain stationary at current point and prevents IOC from counting scanner; when switch is activated, indicator illuminates. Used in conjunction with SET SCANNER.
CLEAR (momentary-contact pushbutton switch)	In step mode only, switch activation clears control sections of core and transistor memory, memory control, and character interface assembly to their quiescent state.
RUN (alternate-action pushbutton-type switch/indicator (white))	Switch activation enables processor unit to perform instructions without interruption (run mode); when switch is activated, indicator illuminates. The following switches are inhibited when RUN switch is activated: SET SCANNER, CLEAR LOAD PA, DISPLAY, and STORE. When RUN switch is not activated (step mode), processor unit performs one operation at a time under control of ADVANCE switch.
ADVANCE (momentary-contact pushbutton switch)	In step mode only, switch activation initiates one processor operation; in run mode, switch activation initiates continuous processor operation.
LOAD PA (momentary-contact pushbutton switch)	In step mode only, switch activation causes contents of KA to be transferred to PA register and displayed on PA indicators.
DISPLAY (momentary-contact pushbutton switch)	In step mode only, switch activation causes contents of memory location specified by KA to be displayed by D indicators.
INTERRUPT (pushbutton switch)	Switch activation sets processing assembly external interrupt flip-flop to "1" to cause an interrupt of a processor operation.
STORE (momentary-contact pushbutton switch)	In step mode only, switch activation causes contents of T keyboard (32-bit console register) to be transferred to memory at address specified by KA.
MEMORY PROT OVRD (alternate-action pushbutton switch/indicator (white))	Not used.
STOP ON STORE ONLY (alternate-action pushbutton-type switch/indicator (white))	Switch activation modifies address stop operation for both the processing assembly and IOC so that a stop occurs on store operations only; when switch is activated, indicator illuminates.
AUTO LOAD (momentary-contact switch)	When depressed, NSPC is activated, provided the processor unit is not in the run mode, and TEST/OPERATE switch on NSPC is in OPERATE position. The AUTO indicator will light when the processor panel CLEAR switch is depressed. The AUTO indicator will go out when NSPC is activated. The TEST indicator of the AUTOLOAD switch is lit only when the NSPC TEST/OPERATE switch is in TEST position.

g. Tape Controller to Processor Panel Interface (fig. FO-3).

Control or indicator	*Function*
RUN indicator (TAPE 1, 2, and 3) (white)	Not used.
HALT indicator (TAPE 1, 2, and 3) (white)	Not used.
FAULT indicator (TAPE 1, 2, and 3) (white)	Not used.
SWITCH ACTION-CONT (3 momentary-contact switches: TAPE 1, 2, and 3)	Not used.
SWITCH ACTION-HALT (3 momentary-contact switches: TAPE 1, 2, and 3)	Not used.
SWITCH ACTION-CLEAR (3 momentary-contact switches: TAPE 1, 2, and 3)	Not used.

h. Panel Lamp Test Function (fig. FO-3). When the LAMP TEST momentary-contact pushbutton on the panel is depressed, all indicator lamps on the panel are illuminated, except that the following switch faceplates do not contain lamps and, therefore, are not illuminated: CLEAR, LOAD PA, ADVANCE, DISPLAY, STORE, SET SCANNER, INTERRUPT, and LAMP TEST.

i. Power Supplies (+16 V DC, −10 V DC, and −27 V DC) (fig. 3-5).

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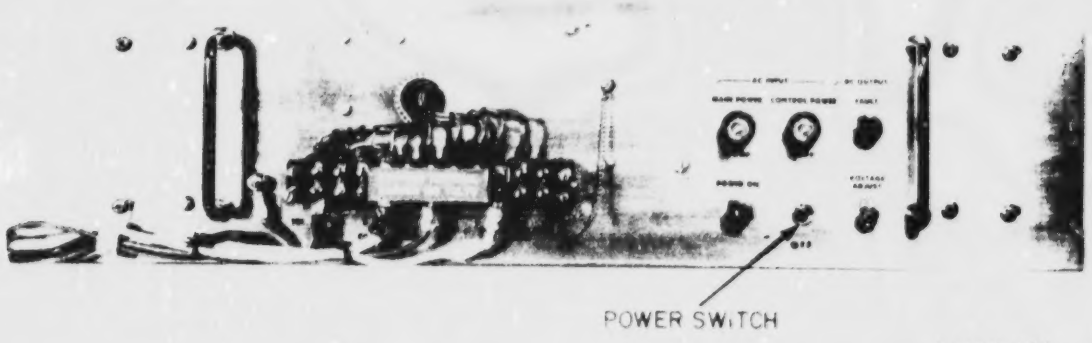

Figure 3-5. Power Supply (+16 V DC, −10 V DC, or −27 V DC) Controls and Indicators.

Control or indicator	*Function*
MAIN POWER blown fuse indicator	When illuminated, indicates that main ac power fuse is open.
CONTROL POWER blown fuse indicator	When illuminated, indicates that fuse for control circuits is open.
FAULT indicator	When illuminated, indicates that an overvoltage or undervoltage condition has occurred, causing removal of ac input voltage to power supply.
VOLTAGE ADJUST screwdriver control	Adjusts output voltage of power supply.
Power switch	Controls application of ac input power to power supply circuits.
POWER ON indicator	When illuminated, indicates that ac power is applied to power supply circuits.

J. Power Supply Controller Panel (fig. 3-6).

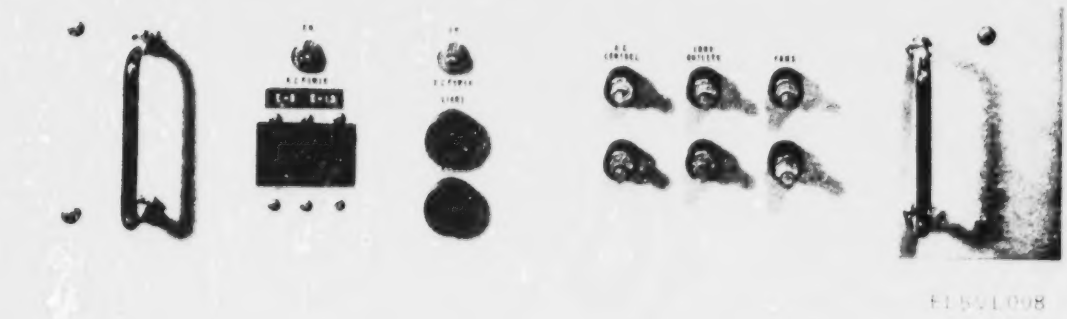

Figure 3-6. Power Supply Controller Panel Controls and Indicators.

Control or indicator	*Function*
AC POWER ON indicator light	When illuminated, indicates that ac power is applied to power supply controller circuits.
DC POWER ON indicator light	When illuminated, indicates that ac primary power is being applied to maintenance console power supplies.
AC CONTROL blown fuse indicator	When illuminated, indicates that fuse for ac control circuits within power supply controller is open.
CONV OUTLETS blown fuse indicator FANS blown fuse indicator	Not used.
FANS blown fuse indicator	When illuminated, indicates that fuse for ac supply to cabinet blowers open.
DC POWER START push button switch	Turns on primary ac power to maintenance console power supplies.
DC POWER STOP pushbutton switch	Turns off primary ac power to maintenance console power supplies.
AC POWER circuit breakers	Controls application of ac input power to power supply controller circuits and AC POWER ON indicator lamp.

k. Clock Panel (fig. 3-7).

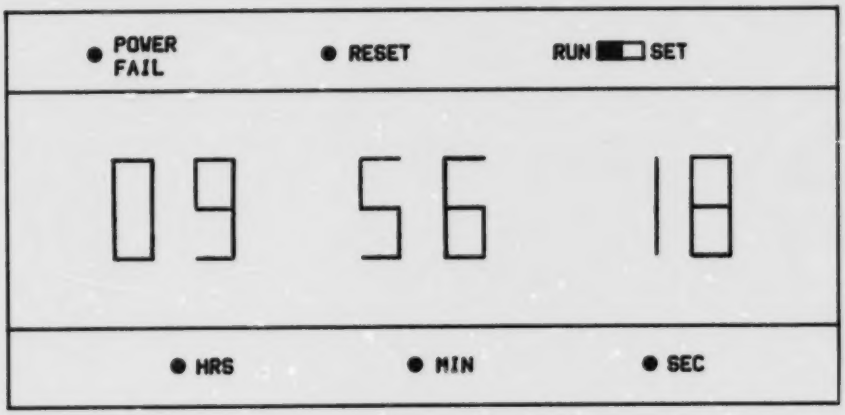

Figure 3-7. Clock Panel, Controls and Indicators.

Control or indicator	*Function*
POWER FAIL indicator light	When illuminated, indicates that a power failure had occurred, and as a result, the indicated time is incorrect. Placing the RUN/SET switch in the SET position extinguishes POWER FAIL light.
RESET switch	Resets the clock readout to 00 hours, 00 minutes, and 00 seconds when pressed.
RUN/SET switch	RUN position is the normal operating position, it allows the clock to increment each second. When the RUN/SET switch is placed in the SET position, the POWER FAIL light is extinguished (if lit), and the clock does not increment.
SEC switch	When pressed, causes the clock readout to increment at the rate of 2 seconds per second.
MIN switch	When pressed, causes the clock readout to increment at the rate of 2 minutes per second.
HRS switch	When pressed, cause the clock readout to increment at the rate of 2 hours per second.

Section II. OPERATION UNDER USUAL CONDITIONS

3-3. Preoperational Checks

a. An offline processor unit with memory bank on tap 0 is required in order to perform preoperational checks on the system status and control console (SSCC) control panels. Therefore, the preoperational checks should be scheduled during a period of time when the least amount of traffic is being handled by the ASC. The release of an operational processor unit to enable preoperational checks to be performed on the OJ-50/FYA-10(V) will be subject to an evaluation of ASC operational requirements and subject to release at the direction of the ASC shift supervisor.

b. Perform preoperational checks on the SSCC control panels as directed in paragraph 3-4.

(1) The preoperational checks for the processor panels are made while interfaced with a serviceable (known good) processor unit which has been placed off line by the ASC shift supervisor.

(2) The offline processor unit is used to determine that panel functions are normal and, therefore, determine that the panel itself is capable of being used as test equipment to assist maintenance personnel in isolation of faults within a defective processor unit.

(3) Processor panel 1 includes provision for sending CLEAR, HALT, and CONT (continue) signals to each of three tape controllers taps.

3-4. Preliminary Starting Procedure

a. Preliminary Control Settings. Set switches of panels (fig. FO-3) as follows:

NOTE

Make sure all interface cables of the system status and control console (SSCC) are connected to the interface receptacles and the SSCC power supplies are operating.

(1) Set all T rocker switches to 0.
(2) Set all KA rocker switches to 0.

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(3) Set RUN switch OFF.
(4) Set TGL AS INST switch OFF.
(5) Set RETAIN INST switch OFF.
(6) Set PROC STOP switch OFF.
(7) Set IOC STOP switch OFF.
(8) Set STOP ON STORE ONLY switch OFF.
(9) Set FAULT ACTION rocker switch OVRD.
(10) Set OPERATE rocker switch to PROC.
(11) Depress CLEAR switch.

b. Lamp Test. The lamp test is made to make certain that all indicator lamps will operate. Depress LAMP TEST switch and observe that all lamps are illuminated while the switch is depressed, except that the following switch faceplates do not contain lamps and, therefore, are not illuminated: CLEAR, LOAD PA, ADVANCE, DISPLAY, STORE, SET SCANNER, INTERRUPT, and LAMP TEST.

c. LOAD PA and KA Switch Test (table 3-1). In this test, the KA rocker switches are activated and a check is made to be certain that the correct PA register is set when the LOAD PA pushbutton is depressed. This test checks all of the logic modules and interface involved in transferring KA rocker switch signals to the processor unit and also checks for proper display of the program address register.

Table 3-1. LOAD PA and KA Switch Test

Step	*Procedure*	*Normal indication*
1	Set controls as listed in paragraph 3-4a.	
2	Depress LOAD PA pushbutton.	PA indicators are out (octal 00000000).
3	Set KA rocker switches to octal 377777. Depress LOAD PA pushbutton.	PA indicators display octal 377777.
4	Set KA rocker switches to octal 000000. Depress LOAD PA pushbutton.	PA indicators display octal 000000.

d. STORE, DISPLAY, and T Switch and D, R, and OAR Register Indicator Test (table 3-2). In this test, data is transferred to various memory locations. Each memory location will have a different data pattern stored in memory. The data patterns are set up so that all logic and interface will be checked for the T rocker switches, D register, and OAR register when the data has been stored and displayed. An additional test uses the same data to check the logic and interface for the R register.

Table 3-2. STORE, DISPLAY, and T Switch and D, R, and OAR Register Indicator Test

Step	Procedure	Normal indication
1	Set controls as listed in paragraph 3-4a.	
2	Set T rocker switches to hexadecimal FFFFFFFF. Depress STORE pushbutton.	D indicators display hexadecimal FFFFFFFF and OAR indicators display octal 000000.
3	Set KA rocker switches to octal 177761 and T rocker switches to hexadecimal 00000000. Depress STORE pushbutton.	D indicators display hexadecimal 00000000 and OAR indicators display octal 177761.
4	Set KA rocker switches to octal 012222 and T rocker switches to hexadecimal 55555555. Depress STORE pushbutton.	D indicators display hexadecimal 55555555 and OAR indicators display octal 012222.
5.	Set KA rocker switches to octal 012525 and T rocker switches to hexadecimal AAAAAAAA. Depress STORE pushbutton.	D indicators display hexadecimal AAAAAAAA and OAR indicators display octal 012525.
6.	Set KA rocker switches to octal 013333 and T rocker switches to hexadecimal FOFOFOFO. Depress STORE pushbutton.	D indicators display hexadecimal FOFOFOFO and OAR indicators display octal 013333.
7	Set KA rocker switches to octal 014444 and T rocker switches to hexadecimal OFOFOFOF. Depress STORE pushbutton.	D indicators display hexadecimal OFOFOFOF and OAR Indicators display octal 014444.
8	Set KA rocker switches to octal 010000 and T rocker switches to hexadecimal OAOAOAOA. Depress STORE pushbutton.	D indicators display hexadecimal OAOAOAOA and OAR indicators display octal 010000.
9	Set KA rocker switches to octal 003000 and T rocker switches to hexadecimal AOAOAOAO. Depress STORE pushbutton.	D indicators display hexadecimal AOAOAOAO and OAR indicators display octal 003000.
10	Set KA rocker switches to octal 000000. Depress DISPLAY pushbutton.	D indicators display hexadecimal FFFFFFFF.
11	Set KA rocker switches to octal 177761. Depress DISPLAY pushbutton.	D indicators display hexadecimal 00000000.
12	Set KA rocker switches to octal 012222. Depress DISPLAY pushbutton.	D indicators display hexadecimal 55555555.
13	Set KA rocker switches to octal 012525. Depress DISPLAY pushbutton.	D indicators display hexadecimal AAAAAAAA.
14	Set KA rocker switches to octal 013333. Depress DISPLAY pushbutton.	D indicators display hexadecimal FOFOFOFO.
15	Set KA rocker switches to octal 014444. Depress DISPLAY pushbutton.	D indicators display hexadecimal OFOFOFOF.

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24.

Table 3-2. STORE, DISPLAY, and T Switch and D, R, and OAR Register Indicator Test—Continued

Step	Procedure	Normal indication
16	Set KA rocker switches to octal 010000. Depress DISPLAY pushbutton.	D indicators display hexadecimal OAOAOAOA.
17	Set KA rocker switches to octal 003000. Depress DISPLAY pushbutton.	D indicators display hexadecimal AOAOAOAO.
	NOTE Steps 18 through 20 load a program to enable data transfers to the R register to be displayed.	
18	Set KA rocker switches to octal 002000 and T rocker switches to hexadecimal 07001004. Depress STORE pushbutton.	
19	Set KA rocker switches to octal 002002 and T rocker switches to hexadecimal 48002800. Depress STORE pushbutton.	
20	Set KA rocker switches to octal 002003 and T rocker switches to hexadecimal 14001000. Depress STORE pushbutton.	
21	Set T rocker switches to hexadecimal 4C000000 and KA rocker switches to octal 002000. Depress LOAD PA pushbutton.	PA indicators display octal 002000.
22	Depress the ADVANCE pushbutton three times in succession.	R indicators display hexadecimal FFFFFFFF.
23	Set T rocker switches to hexadecimal 4C005248. Depress ADVANCE pushbutton four times in succession.	R indicators display hexadecimal 55555555.
24	Set T rocker switches to hexadecimal 4C005554. Depress ADVANCE pushbutton four times in succession.	R indicators display hexadecimal AAAAAAAA.
25	Set T rockers switches to hexadecimal 4C005B6C. Depress ADVANCE push button four times in succession.	R indicators display hexadecimal FOFOFOFO.
26	Set R rocker switches to hexadecimal 4C006490. Depress ADVANCE pushbutton four times in succession.	R indicators display hexadecimal OFOFOFOF.
27	Set T rocker switches to hexadecimal 4C004000. Depress ADVANCE pushbutton four times in succession.	R indicators display hexadecimal OAOAOAOA.
28	Set T rocker switches to hexadecimal 4C001800. Depress ADVANCE pushbutton four times in succession.	R indicators display hexadecimal AOAOAOAO.
29	Set TGL AS INST pushbutton switch to on.	TGL AS INST switch faceplate is illuminated.
30	Set T rocker switches to hexadecimal 06800000. Depress CLEAR pushbutton, then depress ADVANCE pushbutton.	PA indicators display counting activity.
31	Set T rocker switch bit 30 to 1 position.	OAR indicator bit 30 is illuminated ("1").
32	Set T rocker switch bit 31 to 1 position.	OAR indicator bit 31 is illuminated ("1").
33	Depress CLEAR pushbutton.	PA indicators stop counting activity.
34	Set TGL AS INST pushbutton switch to off.	TGL AS INST switch faceplate is no longer illuminated.

e. TGL AS INST Switch and OVF Indicator Test (table 3-3). In this test, an add instruction is performed using the toggle-as-instruction option to cause an overflow condition.

Table 3-3. TGL AS INST Switch and OVF Indicator Test

Step	Procedure	Normal indication
1	Set R rocker switches to hexadecimal 40000000 and KA rocker switches to octal 177761. Depress STORE pushbutton.	
2	Set T rocker switches to hexadecimal 40000000 and KA rocker switches to octal 000000. Depress STORE pushbutton.	
3	Set TGL AS INST pushbutton switch to on.	TGL AS INST switch faceplate is illuminated.
4	Set T rocker switches to hexadecimal 20000000.	
5	Depress CLEAR pushbutton, then depress ADVANCE pushbutton.	OVF (overflow indicator is illuminated.
6	Depress ADVANCE pushbutton once again.	OVF indicator is no longer illuminated.
7	Set TGL AS INST pushbutton switch to off.	TGL AS INST switch faceplate is no longer illuminated.

f. INSTRUCTION REGISTER (IR) Indicator Display Test (table 3-4). In this test, alternate data is stored into an instruction address and an attempt is made to use the data as an instruction. This action causes the alternate data to be transferred to the INSTRUCTION REGISTER (IR). The data pattern is then shifted and another attempt is made to use the data as an instruction which results in another data display in the INSTRUCTION REGISTER indicators.

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Table 3-4. INSTRUCTION REGISTER (IR) Indicator Display Test.

Step	Procedure	Normal indication
1	Set controls as listed in paragraph 3-4*a*.	
2	Set T rocker switches to hexadecimal AAAAAAAA and KA rocker switches to octal 002000. Depress STORE pushbutton.	(This action stores alternate ones and zeros in instruction address.)
3	Depress LOAD PA pushbutton.	PA indicators display octal 002000.
4	Depress ADVANCE pushbutton.	The following INSTRUCTION REGISTER indicators are illuminated ("1"): I, C_2, C_0, R_1, K, X_1, and M.
5	Depress CLEAR pushbutton. Set T rocker switches to hexadecimal 55555555, then depress STORE pushbutton.	(This action shifts ones in same instruction address.)
6	Depress LOAD PA pushbutton.	PA indicators display octal 002000.
7	Depress ADVANCE pushbutton.	The following INSTRUCTION REGISTER indicators are illuminated ("1"): C_3, C_1, R_2, R_0, X_2, and X_0.
8	Depress CLEAR pushbutton.	Also, command fault indicator, CMDF, will be illuminated.

g. RETAIN INST Switch and RUN Switch Test (table 3-5). In this test, an instruction is repeated using the retain instruction option. Also, a check is performed while in run mode to determine that certain other panel switches are inhibited.

Table 3-5. RETAIN INST Switch and RUN Switch Test

Step	Procedure	Normal indication
1	Set controls as listed in paragraph 3-4*a*.	
2	Set RETAIN INST pushbutton switch to on.	RETAIN INST switch faceplate is illuminated.
3	Set T rocker switches to hexadecimal 4C000000 and KA rocker switches to octal 002000. Depress STORE pushbutton.	(This action stores instruction at address 002000.)
4	Depress LOAD PA pushbutton.	PA indicators display octal 002000.
5	Depress CLEAR pushbutton, set RUN pushbutton switch to on, and depress ADVANCE pushbutton.	RUN switch faceplate is illuminated and RUN indicator is illuminated.
6	Set T tocker switches to hexadecimal FFFFFFFF and KA rocker switches to octal 177777.	
7	Depress LOAD PA pushbutton.	There should be no effect observed.
8	Depress STORE pushbutton.	There should be no effect observed.
9	Depress DISPLAY pushbutton.	There should be no effect observed.
10	Depress CLEAR pushbutton.	There should be no effect observed.
11	Depress ADVANCE pushbutton.	There should be no effect observed.
12	Set RUN pushbutton switch to off.	RUN switch faceplate is no longer illuminated. Run indicator is extinguished.

h. SET SCANNER Switch and SCANNER LOCK Switch Test (table 3-6). In this test, the SET SCANNER and SCANNER LOCK switches are checked by observing the results of their action on the OPERAND ADDRESS indicators.

Table 3-6. SET SCANNER Switch and SCANNER LOCK Switch Test

Step	Procedure	Normal indication
1	Set controls as listed in paragraph 3-4*a*.	
2	Open rear door on processor unit frame A; locate levels B and D on logic page of character interface assembly (CIA) (398-6687-1). Connect jumpers from ground to each of the following points: B03-03, B24-12, and D15-05. **NOTE** Installation of jumpers enables the scan counters of the CIA to be gated to the operand address register (OAR) for a visual check of the set scanner operation.	
3	Set SCANNER LOCK pushbutton switch to on.	SCANNER LOCK switch faceplate is illuminated.
4	Depress CLEAR pushbutton and depress SET SCANNER pushbutton.	OPERAND ADDRESS indicators V_7 through V_0 are not illuminated.
5	Set KA rocker switches to octal 000001, then depress SET SCANNER pushbutton.	OPERAND ADDRESS indicators display octal 000001.
6	Set KA rocker switches to octal 000002, then depress SET SCANNER pushbutton.	OPERAND ADDRESS indicators display octal 000002.

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Table 3-6. SET SCANNER Switch and SCANNER LOCK Switch Test—Continued

Step	Procedure	Normal indication
7	Set KA rocker switches to octal 000007 and set RUN pushbutton switch to on.	RUN switch faceplate is illuminated.
8	Depress SET SCANNER pushbutton.	There should be no effect observed.
9	Set RUN pushbutton switch to off.	RUN switch faceplate is no longer illuminated.
10	Depress SET SCANNER pushbutton.	OPERAND ADDRESS indicators display octal 000007.
11	Set SCANNER LOCK pushbutton switch to off.	SCANNER LOCK switch faceplate is no longer illuminated. OPERAND ADDRESS indicators V_7 through V_0 appear to be "on" since scanner is now counting.
12	Set SCANNER LOCK pushbutton switch to on.	SCANNER LOCK switch faceplate is illuminated. OPERAND ADDRESS indicators V_7 through V_0 are illuminated in an undetermined pattern.
13	Set SCANNER LOCK pushbutton switch to off.	SCANNER LOCK switch faceplate is no longer illuminated. OPERAND ADDRESS indicators V_7 through V_0 appear to be "on" since scanner is now counting.
14	Disconnect jumpers (installed in step 2) from B03-03, B24-12, and D15-05 in the character interface assembly of the processor unit; close rear door on processor unit frame A.	

i. FAULT ACTION Switch Test (table 3-7). In this test, a short program is loaded into memory to check the operation of the FAULT ACTION switch in its three positions.

Table 3-7. FAULT ACTION Switch Test.

Step	Procedure	Normal indication
1	Set controls as listed in paragraph 3-4a. NOTE Steps 2 through 4 load a short program to check the FAULT ACTION switch.	
2	Set T rocker switches to hexadecimal 4C020000 and KA rocker switches to octal 002000. Depress STORE pushbutton.	
3	Set T rocker switches to hexadecimal 14001000 and KA rocker switches to octal 002001. Depress STORE pushbutton.	
4	Set T rocker switches to hexadecimal 16801000 and KA rocker switches to octal 000206. Depress STORE pushbutton. NOTE Step 5 forces a 1 bit in a word that was stored as all 0's, to cause a parity error each time the word is transferred from memory.	
5	Open front door on processor unit frame C. On the CSMP (logic page 10, connect a jumper from 0408-2 to 0408-8.	
6	Set FAULT ACTION switch to OVRD (override) position, then depress CLEAR pushbutton.	
7	Set KA rocker switches to octal 002000. Depress LOAD PA pushbutton.	PA indicators display octal 002000.
8	Set RUN pushbutton switch to on.	RUN switch faceplate is illuminated.
9	Depress ADVANCE pushbutton.	Program runs without stopping for parity errors.
10	Set FAULT ACTION switch to INTER (interrupt) position.	Program continues to run, but now the PARITY indicator is "on" to indicate that the parity error is being sensed and that interrupt action is being taken.
11	Set FAULT ACTION switch to STOP position.	Program stops with PARITY indicator brightly illuminated.
12	Set RUN pushbutton switch to off.	RUN switch faceplate is no longer illuminated.
13	Depress CLEAR pushbutton.	PARITY indicator is no longer illuminated.
14	Disconnect jumper (installed) in step 5) from 0408-2 and 0408-8 in the CSMP (logic page 1) of the processor unit; close front door on processor unit frame C.	

j. OPERATE, TGL AS ACW, IOC STOP, PROC STOP, and STOP ON STORE ONLY Switch Test (table 3-8). In this test, a manually stored program is used to check the operation of the TGL AS ACW switch and to check the three positions of the OPERATE switch. The same stored program is then used to check address stops for IOC STOP, PROC STOP, and STOP ON STORE ONLY switches.

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Table 3-8. OPERATE, TGL AS ACW, IOC STOP, PROC STOP, and STOP ON STORE ONLY Switch Test.

Step	Procedure	Normal indication
1	Set controls as listed in paragraph 3-4*a*. **NOTE** Steps 2 through 13 load and store a program which is used to check the operation of the switches.	
2	Set KA rocker switches to octal 002000 and T rocker switches to hexadecimal 4C002800. Depress STORE pushbutton	
3	Set KA rocker switches to octal 002001 and T rocker switches to hexadecimal 48000800. Depress STORE pushbutton.	
4	Set KA rocker switches to octal 002002 and T rocker switches to hexadecimal 4C000400. Depress STORE pushbutton.	
5	Set KA rocker switches to octal 002003 and T rocker switches to hexadecimal 40002808. Depress STORE pushbutton.	
6	Set KA rocker switches to octal 002004 and T rocker switches to hexadecimal 14001008. Depress STORE pushbutton.	
7	Set KA rocker switches to octal 002005 and T rocker switches to hexadecimal 14001000. Depress STORE pushbutton.	
8	Set KA rocker switches to octal 005000 and T rocker switches to hexadecimal 00003000. Depress STORE pushbutton.	
9	Set KA rocker switches to octal 005001 and T rocker switches to hexadecimal A0000000. Depress STORE pushbutton.	
10	Set KA rocker switches to octal 005002 and T rocker switches to hexadecimal A0000800. Depress STORE pushbutton.	
11	Set KA rocker switches to octal 006000 and T rocker switches to hexadecimal C8002805. Depress STORE pushbutton.	
12	Set KA rocker switches to octal 006001 and T rocker switches to hexadecimal A8004000. Depress STORE pushbutton.	
13	Set KA rocker switches to octal 006002 and T rocker switches to hexadecimal C8002804. Depress STORE pushbutton.	
14	Set OPERATE switch to BOTH position.	
15	Set KA rocker switches to octal 002000. Depress LOAD PA pushbutton.	PA indicators display octal 002000.
16	Depress CLEAR pushbutton, then depress ADVANCE pushbutton four times in succession.	PROC (processor) indicator illuminates when ADVANCE pushbutton is depressed for the first time and extinguishes on the fourth time.
17	Continue to depress and release the ADVANCE pushbutton several times while observing PROC indicator.	PROC indicator illuminates on every other actuation of ADVANCE switch. (This action indicates that both the input-output control assembly and the processor are alternately using the common data section.)
18	Set OPERATE switch to IOC position.	
19	Continue to depress and release the ADVANCE pushbutton several times.	PROC indicator is no longer illuminated at any time. (This indicates that only the input-output control assembly is operating.)
20	Set OPERATE switch to PROC position.	
21	Continue to depress and release the ADVANCE pushbutton while observing PROC indicator.	PROC indicator illuminates and remains illuminated throughout operation of ADVANCE pushbutton. (This indicates that only the processor unit is operating.)
22	Set OPERATE switch to BOTH position, and set RUN pushbutton switch to on.	RUN switch faceplate is illuminated.
23	Depress ADVANCE pushbutton.	
24	Set KA rocker switches to octal 001000.	
25	Set PROC STOP switch to on.	PROC STOP switch faceplate is illuminated. After a short delay, PROC and ADS indicators are illuminated to indicate processor unit has stopped.
26	Set KA rocker switches to octal 002000, and set PROC STOP switch to off.	PROC STOP switch faceplate is no longer illuminated.
27	Depress ADVANCE pushbutton.	Program resumes (RUN indicator illuminates).
28	Set PROC STOP switch to on.	PROC STOP switch faceplate is illuminated. After a short delay, PROC and ADS indicators are illuminated.
29	Set STOP ON STORE ONLY switch to on.	STOP ON STORE ONLY switch faceplate is illuminated.
30	Depress ADVANCE pushbutton.	Program resumes. Observe that processor unit does not stop. (ADS indicator is not illuminated.)
31	Set KA rocker switchs to octal 001000.	After a short delay, PROC and ADS indicators are illuminated to indicate processor unit has stopped.

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Table 3-8. OPERATE, TGL AS ACW, IOC STOP, PROC STOP, and STOP ON STORE ONLY Switch Test—Continued.

Step	Procedure	Normal indication
32	Set both PROC STOP and STOP ON STORE ONLY switches to off.	PROC STOP and STOP ON STORE ONLY switch faceplates are no longer illuminated.
33	Depress ADVANCE pushbutton.	Program resumes.
34	Set KA rocker switches to octal 010000.	
35	Set IOC STOP switch to on.	IOC STOP switch faceplate is illuminated. Program will stop with PROC indicator off and ADS indicator illuminated.
36	Set IOC STOP switch to off.	IOC STOP switch faceplate is no longer illuminated.
37	Depress ADVANCE pushbutton.	Program resumes.
38	Set KA rocker switches to octal 006000.	
39	Set IOC STOP switch to on.	IOC STOP switch faceplate is illuminated. Program will stop with PROC indicator off and ADS indicator illuminated.
40	Set STOP ON STORE ONLY switch to on.	STOP ON STORE ONLY switch faceplate is illuminated.
41	Depress ADVANCE pushbutton.	Program resumes. (RUN indicator illuminated.)
42	Set KA rocker switches to octal 010000.	Program will stop with PROC indicator off and ADS indicator illuminated.
43	Set both STOP ON STORE ONLY and IOC STOP switches to off.	STOP ON STORE ONLY and IOC STOP switch faceplates are no longer illuminated.
44	Set RUN switch to off.	RUN switch faceplate is no longer illuminated.
45	Set OPERATE switch to PROC position, then depress CLEAR pushbutton.	

3-5. Operating Procedure

a. Starting the Equipment. To turn on power to the system status and control console, proceed as follows:

(1) Set the AC POWER circuit breakers on the power supply controller panel (fig. 3-6) to the ON position. The AC POWER ON indicator shall illuminate.

(2) Place all power switches on the individual power supplies (+16 V dc, −10 V dc, and −27 V dc) in the up (on) position (fig. 3-5).

(3) On the power supply controller panel, depress the DC POWER START pushbutton. The DC POWER ON indicator shall illuminate. The POWER ON indicator on each power supply shall illuminate.

b. Basic Operating Procedures. Information for the operation of the power supplies, power supply controller, processor panels, fault indicator panel, system autoload module panel, and configuration control panel is provided in this section. The operational modes of the intercom/paging unit, system command terminals, and video display units are discussed in the respective individual manuals listed in appendix A.

c. Processor Panels. The processor panels are used for operation and control of the standby processor unit or any offline processor unit. This is accomplished by displaying the contents of various processor registers, injecting test words into processor registers, and controlling and displaying specific operational modes of the processor unit. In addition, each processor panel includes provisions for controls and indicators for certain peripheral devices which may be used during maintenance programs or procedures. Detailed operating procedures are given in TM 11-5895-406-15/1.

NOTE

Do not connect a processor panel to an on-line processor. The processor panel must first be connected to an off-line processor. The processor can then be switched on line with the processor panel connected.

d. Touch-Activated (TA) Switches. The system autoload module panel, fault indicator panel, and configuration control panel contain touch-activated (TA) switches. TA switches are capacitively coupled, logic controlled switches (most with numerical displays). The use of TA switches is as follows:

(1) A light touch to the bottom of the switch (or below the display) will activate the switch (and count up the display by one digit).

(2) Touch and hold the bottom of the switch to cause the display to auto-count up at the rate of three digits per second.

(3) The maximum count that each switch can reach is a preset logic function. Once the maximum count is passed, the display will automatically reset to 0.

(4) A light touch to the top of the switch (above the display) will activate the switch and manually reset the display to 0.

e. System Autoload Module Panel (fig. 3-1). The system autoload module (SAM) panel is used to control the starting of a 102 processor for reloads and console-initiated restarts. Manual reloads (less functions 4 and 5) and manual restarts are required only in the event of a major malfunction of the SAM. Manual reloads are performed as before. Manual re-

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starts are still initiated by a processor panel. Supervisory commands may be entered from the SCT to initiate a restart. However, the REST 09 command will require mounting a program library disc (PLD) on the correct DEC pack disk cartridge drive prior to the command.

f. Fault Indicator Panel (fig. FO-2). The fault indicator panel is used to provide hardware status. An ERROR RESET switch is located on the panel to enable the clearing of the fault indicators. No other operator actions are required or initiated by the fault indicator panel. Refer to section I, paragraph 3-2b for indicator definitions.

g. Configuration Control Panel (fig. 3-2). The configuration control panel is used for both monitor control and configuration switch controller (CSS) control. The monitor control switches are used to first select the desired message processor (MP) and then select the monitor to be connected to the message processor. The selected monitor is then started and connected to the selected MP. The remaining switches are for the manual reconfiguration.

h. Automatic Reload/Restart. The operator-initiated automatic reload/restart is controlled by the SAM panel. Proceed as follows to initiate either a reload or a restart:

NOTE

Refer to DCAC 310-D70-32 for a detailed description of the reload/restart procedure and printouts.

(1) If the BSS processor is not running the operational software, mount the operational program library disk (PLD) DEC pack in the selected BSS as DLO.

(2) Press the CNTRL-HALT, CLR, and CNTRL-BOOT keys on the operator's console of the PDP-11/34C. Observe the startup and ending notice printouts on the LA36 tty set.

(3) On the SAM panel, touch the R/R (reload/restart) switch to select *1* for reload or *2* for restart.

(4) On the SAM panel, touch the PNL (processor panel) switch to select panel *1* or *2*.

(5) On the SAM panel, touch the BSS (bulk storage system) switch to select BSS *1* or *2*.

(6) On the SAM panel, touch the SCT (system command terminal) switch to select SCT *1* or *2*.

(7) For reload operation only, on the SAM panel, touch the HIST switch to select *0* for no history balance or *1* for a history balance.

(8) On the SAM panel, touch the CSC (configuration switch controller) switch to select CSC *1* or *2*.

(9) On the configuration control panel, touch the MP (message processor) switch to select MP *1* through *6*.

(10) On the configuration control panel, touch the MON SEL (monitor select) switch to select monitor *1* or *2*.

(11) On the SAM panel, touch the ENABLE switch. This will enable the NSRP and both amber indicators will flash.

(12) On the SAM panel, touch the START switch and ensure the yellow ENABLE indicators extinguish and the green indicator on the START switch illuminates.

(13) After the successful restart or reload is completed, the green indicator will extinguish. An unsuccessful attempt will illuminate the red indicator on the START switch and require repeating steps (1) through (13).

(14) Response at the SCT is prompt message to load date and time.

(15) On the SCT keyboard, type the military date and time.

(16) After a prompt message on the SCT, type information for mass memories. After a second prompt message, type information for the processors, line terminal buffers, SCT, and configuration switch controller.

(17) After a prompt message from the bulk storage subsystem (BSS) at the LA36 tty set, type the disk drive numbers of history packs A and B.

(18) When the BSS has opened the required files, the system will come up in cycle stall.

(19) At the prime MTSS VDU, press function key F11 to activate the VDU and latch onto the scanner.

(20) On the SCT keyboard, press PFK4 to take the system out of cycle stall.

CAUTION

A system failure can occur if operation of the message processor is not halted while an offering processor is powered up.

i. Power Up Offline Processor. Power up the offline processor as follows:

(1) Connect the processor panel to the message processor (MP).

(2) Name the MP its own successor.

(3) Stop the MP at the top of cycle (0/1200).

(4) Power up the offline processor as described in TM 11-5895-406-15/1.

(5) Using the processor panel, perform a manual restart 02 for the MP as follows:

(a) Set T toggles to H/00000002.

(b) Set KA toggles to 0/1201.

(c) Press the CLEAR, LOAD PA, RUN, and ADVANCE buttons.

(d) Restart 02 printouts will indicate that the processor is operating.

j. VDU Display. Operation of the VDU display is controlled by the VDU keyboard. Using the VDU

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keyboard, data can be displayed, checked, and if necessary, changed or corrected, and transferred to the processor. Refer to DCAC 310-70-32 for detailed operating procedures.

(1) *Display areas.* Display lines 1-20 contain any large (over 4 lines) displays. The alarms display, and the configuration stat represent a large display. Both of these displays cannot appear at the same time. A requested configuration stat will overlay the alarms display if it is present. Display lines 21-24 contain short displays (4 lines or less). Line readouts and stats 0-4 are of this type. Display line 25 contains various command and system messages. The entire screen may contain at the same time, a large message (lines 1-20), short messages or readouts (lines 21-24), and a line 25 message. The normal state of the entire display (display lines 1 through 20) is reverse video.

(2) *Alarm indications.* Alarms are indicated as follows:

Alarm	*Display*
Alarming line	Normal blinking
Alarming line is a readout	Normal continuous
Out-of-service line	Dim blinking
Out-of-service line acknowledge	Dim continuous
Major or processing alarm	Normal blinking

(3) *Display readout.* The readout area of the display (lines 21 through 24) is used for alarming line and select line functions and is under normal attribute control. The specified line number and any faults (loss of carrier, etc.) are in a blinking state. The configuration status is updated automatically at every VDU that has it displayed. Whenever a status update occurs, a STAT PFK6 blinking message is displayed on the 25th line of the VDU (even if the configuration status is not being displayed on the VDU when the update is received). The operator must then press program function key (PFK) F6 to acknowledge the configuration change. Further data entry inputs cannot be made until the update message is acknowledged. Display line 25 indications during command processing are shown in table 3-9 for the following example:

Cycle Channel 35 [035(PFK2)]

(4) *Data entry.* All text data and command entries are made using the VDU keyboard, numeric keypad, and 16 PFK's. Text entries are used for DCA-55 reports in the edit mode of operation. This mode is entered by pressing PFK3. The screen is cleared except line 25 which reads EDIT MODE. DCA-55 messages and/or commands can now be entered. After each DCA-55 input, the operator must wait until the SEND NEXT message appears on the screen. Exit edit mode by pressing PFK5. Refer to table 3-10 for the function of the PFKs when the VDU is in the text editor mode.

Table 3-9. VDU Display Line 25 Indications.

Function	Indication
Command echo back	"035 PFK 2" in normal display mode
Valid command response message	"Cycle Channel 035" in normal display mode
Invalid command response message	"Invalid 435 PFK 2". Word "Invalid" is blinking
Command done indication (no response type of command)	"Cycle Channel 035". Entire message is in reverse video mode
Invalid command (detected by MP) response message	"Cycle Channel 035". Entire message is blinking
Configuration status update	"STAT PFK 6" is blinking

Table 3-10. VDU Text Editor Mode Program Function Keys (PFK).

PFK	Function (PFK unshifted)	Function (PFK shifted)
F1	Delete character	Spare
F2	Insert line	Delete line
F3	Memory erase	Cursor erase
F4	Not used	Not used
F5	Not used	Not used
F6	Transmit text to host computer (LSI 11)	Spare
F7	Define block	Spare
F8	Copy block	Spare
F9	Cancel block	Spare
F10	Delete block	Spare
F11	Move block	Spare
F12	End paragraph	Spare

k. VDU Programed Function Keys. Operation of the 16 programed function keys is accomplished by merely depressing a single function key. When depressed, each key causes a unique four-character sequence to be transmitted to the processor. The form of the four-character sequence is EOT, ESC, "N", EOT; when "N" is the ASCII code for the number on top of the key. Program recognition of the ESC (escape) control character indicates that the following character is to be interpreted outside of the normal

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code set. The processor then executes preprogramed instructions corresponding to the key number. The 16 keys are used in both the shifted and unshifted modes, giving a total of 32 functions. Table 3-11 identifies the functions selected by the keys.

NOTE

Shifted programed key functions must be used with care as they may affect normal operation of the MTSS.

Table 3-11. VDU Programmed Function Keys.

Key	Function (key unshifted)	Function (key shifted)
F1	Cycle channel	Start scan
F2	Status request	Stop scan
F3	DCA-55 request	Start exception reporting
F4	Cancel DCA-55	Spare
F5	Exit text edit mode	Spare
F6	Configuration stat change acknowledge	Stop exception reporting
F7	Alarming line display request	Spare
F8	Alarming line readout	Inhibit line scanning
F9	Major alarms system reset	Spare
F10	Acknowledge out-of-service lines	Spare
F11	Scanner control	Reset scanner
F12	Video control	Readout line override
F13	SAC disconnect all switches	All channel clear
F14	Select audio switch	Acknowledge processing alarms
F15	Select black switch	Spare
F16	Select red switch	Reset SAC

l. VDU Command Formats. Commands are entered using the numeric keypad and the programmed function key. The major command component is the selected PFK. When an individual channel (circuit line) is the object of a command, a command parameter which is the three digit line number (such as 035) is entered on the numeric keypad before pressing the selected PFK. The function of some PFK's is modified by the use of a component separator (decimal point on numeric keypad) and a command modifier which is one numeric key before pressing the PFK. For instance, a STAT 2 request is "2 (PFK2)." Some commands such as a STAT0 request include all command components (035.0 (PFK2)). Table 3-12 shows the keying sequence of each command.

3-6. Stopping Procedure

To turn off power to the system status and control console (SSCC), proceed as follows:

a. Depress the DC POWER STOP pushbutton (fig. 3-6) and ensure that the DC POWER ON indicator extinguishes. Ensure the POWER ON indicator on each supply extinguishes.

b. Place the AC POWER circuit breakers, on the power supply controller, in the OFF position and ensure that AC POWER ON indicator extinguishes.

c. Place the power switches, on the individual power supplies (+16 V dc, −10 V dc, and −27 V dc), in the OFF position and ensure the associated POWER ON indicators extinguish.

Table 3-12. VDU Command Keying Sequence.

Command (CMD)	Function	Sequence
Cycle channel	Line YYY is alternately put out of service and back into service. The line must be in service when this command is sent.	YYY (PFK1)
Stat requests	*a.* STAT0 Single destination backlog, displayed on lines 21 through 24.	NNN.0 (PFK2)
	b. STAT1 Single line blacklog, displayed on lines 21 through 24.	NNN.1 (PFK2)
	c. STAT2 Oldest assigned serial number (ASN), displayed on line 21.	2 (PFK2)
	d. STAT3 Single line backlog, language media format (LMF) displayed on lines 21 through 24.	NNN.3 (PFK2)
	e. STAT4 Single destination backlog LMF displayed on lines 21 through 24.	NNN.4 (PFK2)
	f. CONFIG System configuration stat displayed on lines 1 through 20.	(PFK2)
DCAC-55 request	The display is cleared. DCAC-55 REQUEST is displayed on line 25. DCAC-55 commands and data may then be entered.	(PFK3)

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Table 3-12. VDU Command Keying Sequence—Continued.

Command (CMD)	Function	Sequence
Cancel DCAC-55	The current DCAC-55 narrative message is canceled. An acknowledgement message is displayed.	(PFK4)
Exit text edit mode	The display is cleared. Normal commands can be entered.	(PFK5)
Configuration stat change acknowledgement	A blinking STAT PFK6 message on line 25 indicates a configuration stat change message has been received. PFK6 must be pressed before any more commands can be entered.	(PFK6)
Alarming line display request	Displays alarm status on lines 1 through 20. Major system alarms are displayed on lines 1 through 3. System processing alarms are displayed on line 4. Communication lines 0 through 223 are displayed on lines 6 through 20.	(PFK7)
Alarming line readout (specific)	The status of line YYY is displayed on lines 21 through 24.	YYY (PFK8)
Alarming line readout (automatic)	The highest priority line that is alarming is read out. If PFK8 is pressed again, the next highest priority line that is alarming is read out. If no lines are alarming, line 25 displays ALARMS DONE.	(PFK8)
Major systems alarms reset	Any unacknowledged (normal, blinking) major system alarms are acknowledged (normal, nonblinking).	(PFK9)
Acknowledge out of service lines	The out of service lines (which are dim and blinking) are set to dim and steady.	(PFK10)
Scanner control (only from MTSS VDU)	The scanner will respond to commands from this LSI-11/2 only.	(PFK11)
Video control (only from prime MTSS VDU)	Initializes both SSCC VDU's and causes them to display ENTER REQUEST. The SSCC operator may then enter commands.	(PFK12)
Disconnect all SAC switches	SAC is disconnected from all interfaces. All indicators on manual selection control panel are extinguished.	(PFK13)
Connect audio switch (specific)	Connects line YYY to MTC at RAU	YYY (PFK14)
Connect audio switch (implied)	Connects the line specified in a preceding SAC command to MTC at RAU.	(PFK14)
Connect black switch (specific)	Connects line YYY to MTC at black remote switcher.	YYY (PFK15)
Connect black switch (implied)	Connects the line specified in a preceding SAC command to MTC at black remote switcher.	(PFK15)
Connect red switch (specific)	Connects line YYY to MTC at red remote switcher.	YYY (PFK16)
Connect red switch (implied)	Connects the line specified in a preceding SAC command to MTC at red remote switcher.	(PFK16)
Start exception report	Scanner starts exception reporting.	Shifted (PFK3)
Stop exception report	Scanner stops exception reporting.	Shifted (PFK6)
Inhibit line scanning	Inhibit scanning of line YYY.	YYY shifted (PFK8)
Reset scanner	All new existing alarms wil be reported by scanner.	Shifted (PFK11)
Alarming line readout override	Clears programs sensed errors for line YYY. For this command to be valid, one SSCC VDU must have had a readout for line YYY.	YYY shifted (PFK12)
All channel clear (only from SSCC)	All out-of-service lines changed to in-service. Processing alarm backlogs remain.	Shifted (PFK13)
Acknowledge processing alarm (only from SSCC)	Any system backlog alarms unacknowledge (normal, blinking) will be acknowledged (normal, non-blinking). For "printout waiting", or "high priority message in system" the alarm (blinking) will be cleared.	Shifted (PFK14)
Rest SAC	SAC interface is initialized.	Shifted (PFK16)

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CHAPTER 4

FUNCTIONING OF EQUIPMENT

Section I. OVERALL DESCRIPTION

4-1. Introduction

The system status and control console (SSCC) (fig. 4-1) enables overall supervision of the operation and maintenance of the ADMS. The SSCC contains a system autoload module (SAM) panel, a fault indicator panel, a configuration control panel, a SSCC logic board, two video display units (VDU's) with keyboards, an intercom panel, two processor panels, and two message consoles (SCT's).

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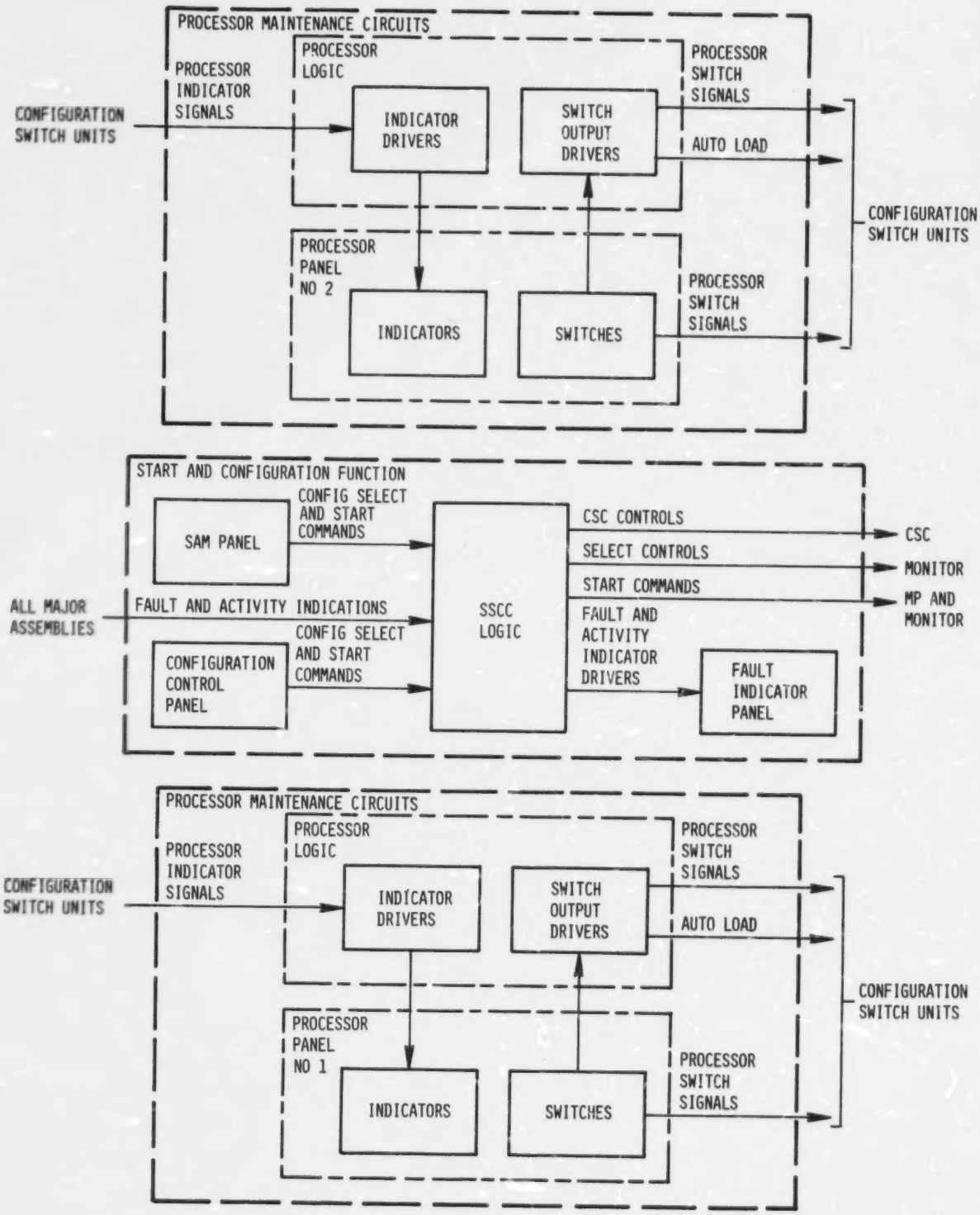

Figure 4-1. SSCC, Overall Block Diagram.

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a. The SAM panel controls the autoloading of a selected 102 processor unit for reloads or console-initiated restarts. Touch-activated switches on the SAM panel allow selection of an SCT, BSS (bulk storage subsystem), history pack, CSC (configuration switch controller) and reload/restart. The operator may start a 102 processor by depressing the ENABLE switch and then the START switch. This action will also latch the selected CSC. A yellow ENABLE light will flash when the SAM is enabled and go out when the SAM is started. The green START light will be illuminated while the selected processor's nonvolatile stored program controller (NSPC) is active and running. Any error condition that would cause the NSPC to halt will extinguish the green START light and illuminate the red START light.

b. The fault indicator panel provides hardware status indications for each of the major units of the ADMS group. Fault and unit-unavailable indicators are provided for processor memories, mass memories, CSC's, and BSS units. Indicators are also provided to display the halt, parity, command fault, and step status of each 102 processor. Power supply failure indicators are provided for the configuration control and sensing unit cabinet.

c. The configuration control panel contains switches and indicators which are used to manually configure the ADMS.

d. The SSCC logic board contains all the logic and interface functions from the SAM panel, fault indicator panel and configuration control panel.

e. The video display units (VDU's) and associated keyboards provide channel and subsystem status. The VDU's are updated by a micro-processor (LSI-11/2) which is part of the monitor test and status subsystem. The two VDU's are capable of displaying channel status, subsystem status, and any other requested system stats. This soft stat feature reduces printer traffic and provides the operator with a fast, easy means of checking system status. This feature also reduces operator movement requirements. The printer need only be used for required stat recording. The two VDU's are functionally interchangeable and identical in capabilities. The channel and system status displays are page functions, and any page can be selected by the operator on either VDU. The operator is able to swap VDU's and carry over the channel status if so desired simply by selecting the appropriate page. Channel status alarms are on an exception basis and are generated and updated by the software without operator action.

f. The intercom panel is used for intra-ADMS communication and has a hands-free operation capability. For a detailed description of the intercom panel, refer to TM 11-5895-416-15.

g. The two processor panels are used to manually address and operate any selected offline 102 processor unit.

h. The message consoles are used for man/machine interface with the 102 processor units. One message console is always interfacing with the message processor (MP) unit. The other message console can be used to interface with any selected offline 102 processor.

4-2. Start and Configuration Function

The logic for this function (SSCC logic) is contained in drawing 520484. The following paragraphs provide a detailed description of the SSCC logic and describe the interaction with the SAM panel, the configuration control panel, and the fault indicator panel. Descriptions of the individual integrated circuits are contained in section II of this chapter.

a. SAM Start (fig. FO-4, 4-2 and 4-3). Initial contact with the ENABLE switch causes a series of negative pulses (SAM ENA SW) which trigger single-shot (SS) 1E6A. Releasing the ENABLE switch halts the negative pulses, which halts the retriggering of SS 1E6A, allowing it to time out. The positive-going edge of the SS 1E6A output sets ENABLE FF 1D6A. The resultant high ENABLE causes the yellow ENABLE indicator to flash and enables gate 1D3A. The other input to the gate is determined by the CSC select. When a CSC is not selected (0), both the CSC1 and CSC 2 signals are low, thus keeping the INH SAM low and inhibiting a start. When a CSC 1 or 2 is selected, the corresponding CSC 1 or 2 signal is high, enabling the manual connect logic (MANUAL SS 2E4B) and removing the inhibit from SS 1E5A and 1D4B by setting the INH SAM high. Contact with the START switch triggers RETRIG SS 1E5A. When the single-shot times out, the positive-going edge of the output triggers SS 1D5A, which sets RLS FF 1C5A (since the D input to 1C5A was high, the 1 output goes high and the 0 output goes low). The RLS FF 1C5A is cleared by a low CLR RLS generated by the counters on sheet 4, which act as a 250 ms time delay. The high RLS is gated with the MON 1 and 2 SEL enables and routed to the selected monitor. The negative-going edge of the RLS triggers SS 1D4B. The high SSRSS output is gated with the high INH SAM, sending a high ACTIVATE NSPC 1 or 2 to a 102 processor via the selected monitor. The ACTIVATE NSPC (nonvolatile stored program controller) signal initiates the SAM startup sequence in the 102 processor. The low SSRSS sets ACTIVE FF 1E2A (the 1 output goes high) and the lagging (positive going) edge fires SS 1E6A, which toggles FF 1D6A (ENABLE output goes low). The low ENABLE turns off the yellow

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ENABLE indicator and sets the INH SAM low, inhibiting SS 1E5A and 1D4A. The ACTIVE FF remains set (1 output high), thus enabling gates 1C2A and 1C2B, during the entire SAM startup sequence. If a failure occurs in the SAM startup sequence, the selected monitor routes the fault indication (FAULT M1 or FAULT M2 goes high) to gate 1E2B or gate 1E1A, resulting in turning on the red START indicator. If a fault is not received, the FAULT M1 and FAULT M2 signals are low, resulting in a high NSPC FAULT which turns on the green START indicator and holds off the red START indicator. When the processor has completed the SAM startup sequence and received the first and second verification characters from the monitor, it routes an ROCM (ROCM M1 or ROCM M2 goes high, momentarily) via the selected monitor to gate 1E1C or gate 1E1B. This results in a low output from gate 1D1A. When the output of 1D1A returns high, the ACTIVE FF is reset, disabling gate 1C2A, which turns off the green START indicator.

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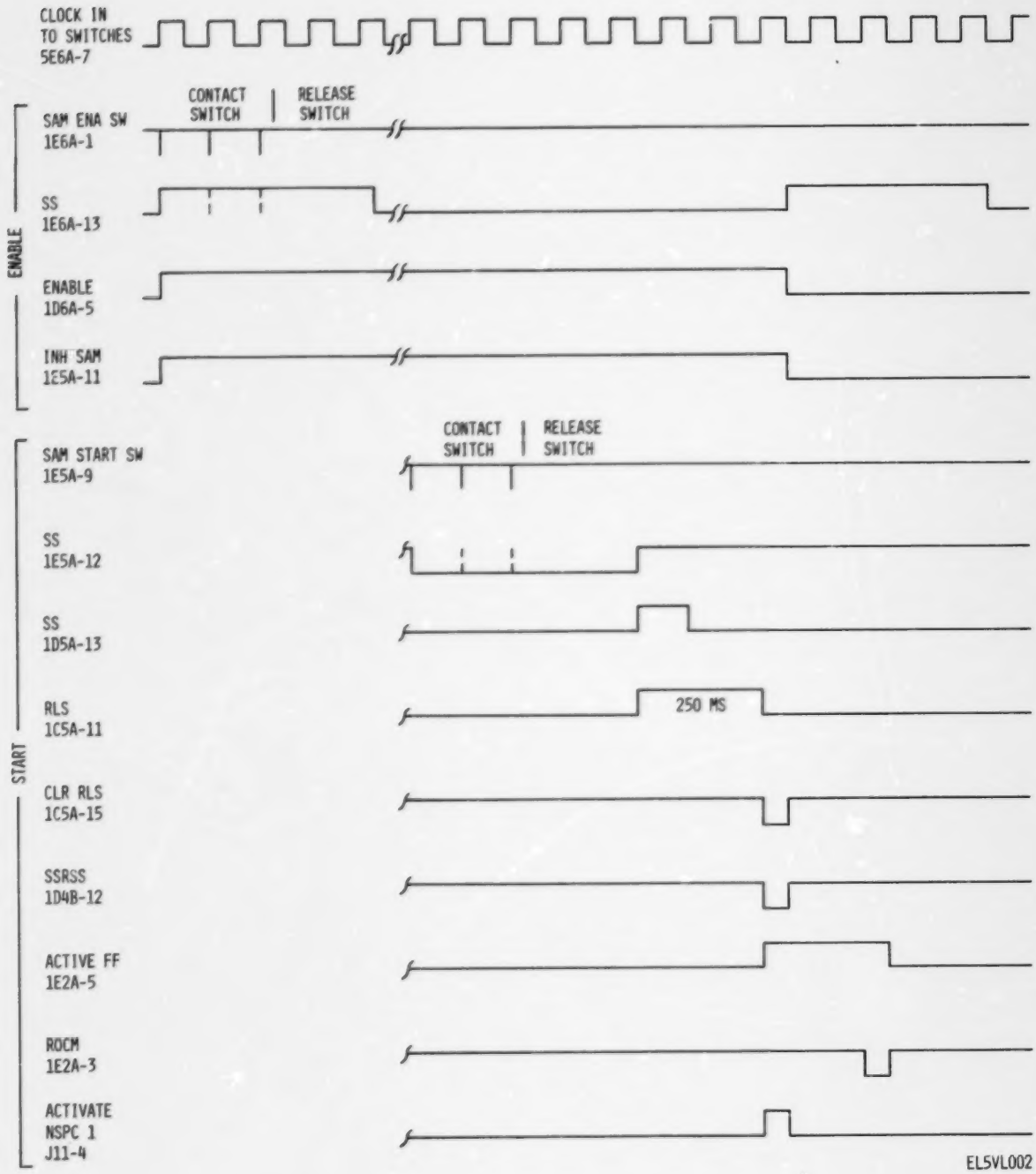

Figure 4-2. SAM Start Timing.

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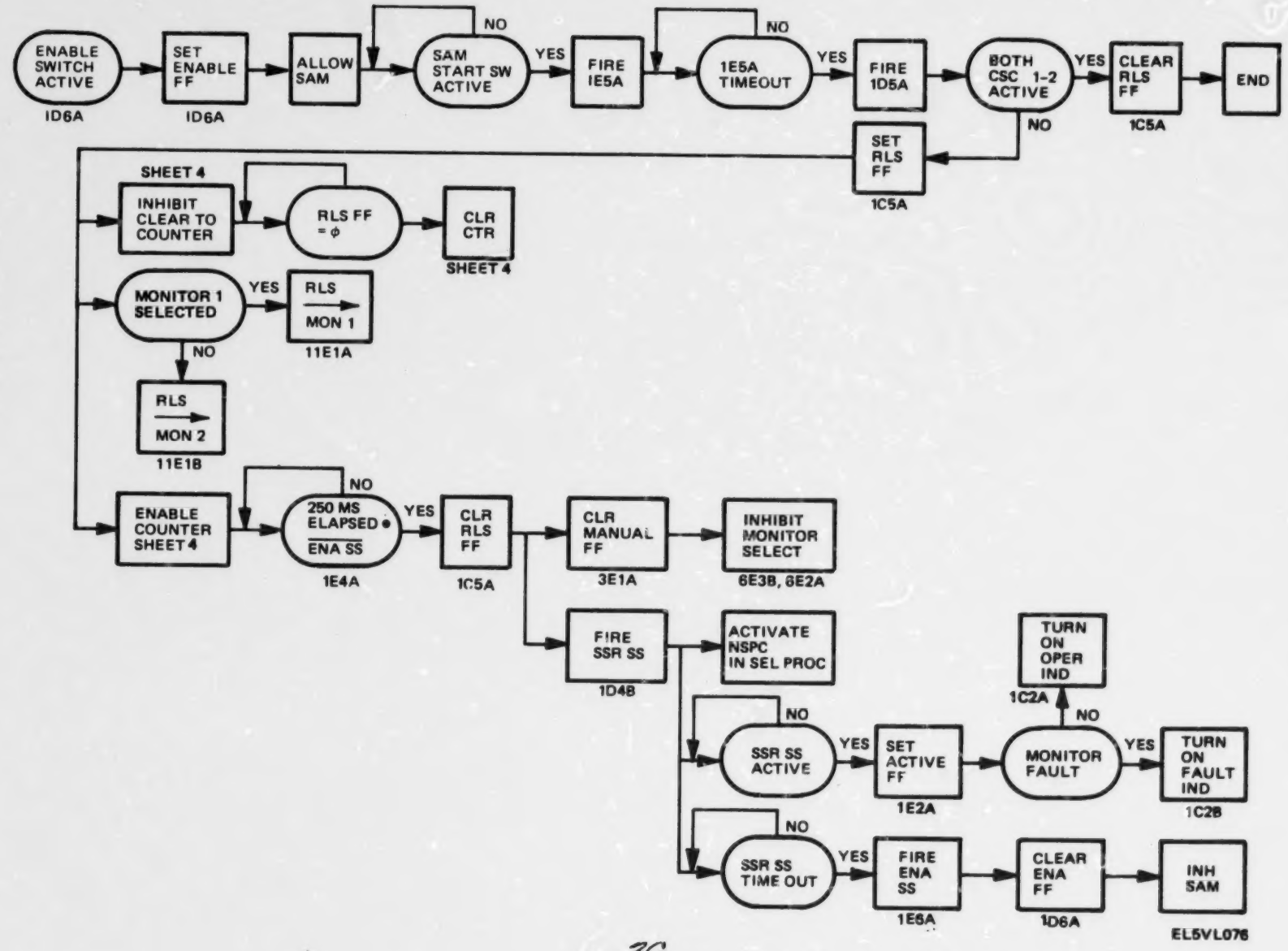

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Figure 4-3. SAM Start, Flow Chart.

b. Manual Connect (fig. FO-4 and 4-4). Initial contact with the CON CSC switch causes a series of negative pulses (CONNECT CSC SW) which trigger MANUAL single-shot 2E4B. The 0 output (MANUAL SS) sets MANUAL FF 3E1A 1 output high, which routes a high MANUAL CONNECT to the selected monitor. Releasing the CON CSC switch halts the negative pulses from the switch, which halts the retriggering of MANUAL SS 2E4B, allowing it to time out. When the single-shot times out, the 1 output (MANUAL SS) goes low, which triggers SS 1D5A. The high output of SS 1D5A sets RLS FF 1C5A (since the D input was high, the 1 output goes high and 0 output goes low). RLS FF 1C5A is cleared by a low CLR RLS, generated by the counters on sheet 4, which act as a 250 ms time delay. The high RLS is gated with the MON 1 and 2 SEL enables and routed to the selected monitor. SS 1D4B is inhibited from firing by a low INH SAM. When the 0 output from the RLS FF 1C5A returns high (reset), MANUAL FF 3E1A is reset. This removes the high MANUAL output from gates 6E3B and 6E2A and halts the high MANUAL CONNECT to the selected monitor.

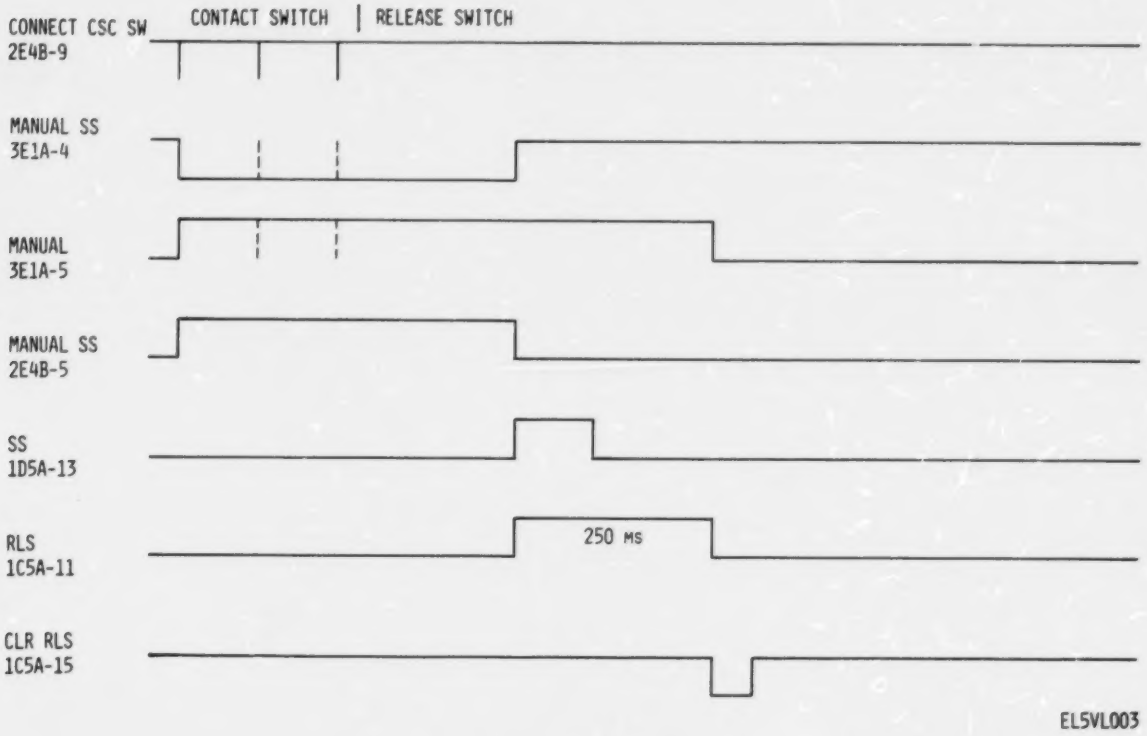

Figure 4-4. Manual Connect Timing.

c. Monitor Selection (fig. FO-4). Contact with the MON SEL switch causes a switch of negative pulses (MON SEL SW), which trigger SS 2E4A. The output of SS 2E4A toggles FF 2D4A. Each time SS 2E4A is fired (by contact with the MON SEL switch), FF 2D4A is toggled, reversing the state of the outputs. When the 1 output (MON 1 SEL) is high, a low MON 1 SELECT is routed to monitor 1, the MON SEL 1 indicator lights, and a high MON 1 SEL is routed to gates 1D2B, 1D1A, 11E1A/11D2D, 6E3B, and 2D5A. To select monitor 2, contact is made with the MON SEL switch, which triggers SS 2E4A, which toggles FF 2D4A. This results in the 1 output (MON 1 SEL) going low and the 0 output (MON 2 SEL) going high. Therefore the MON SEL 1 indicator goes out, MON SEL 2 indicator goes on, a low MON 2 SELECT is routed to monitor 2, and a high MON 2 SEL is routed to gates 1D2B, 1D1A, 11E1B/11D1A, 6E2A, and 2D6B.

d. Processor Failure (fig. FO-4). During processor operation, the monitor continuously checks for proper processor operation. The monitor must receive major and minor DVCW's (device control words) from the processor within specified time periods. If the DVCW's are not received, M1 FAULT or M2 FAULT goes high, which lights the red START MON 1 or START MON 2 indicator.

e. Fault Indicator Panel Logic. This logic (drawing

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520484, sheets 14 through 21) provides the drive circuits for the LED's on the fault indicator panel. All of the fault and U/U (unit available) drive circuits are very similar. A typical circuit is shown in figure 4-5 and described in the following paragraphs.

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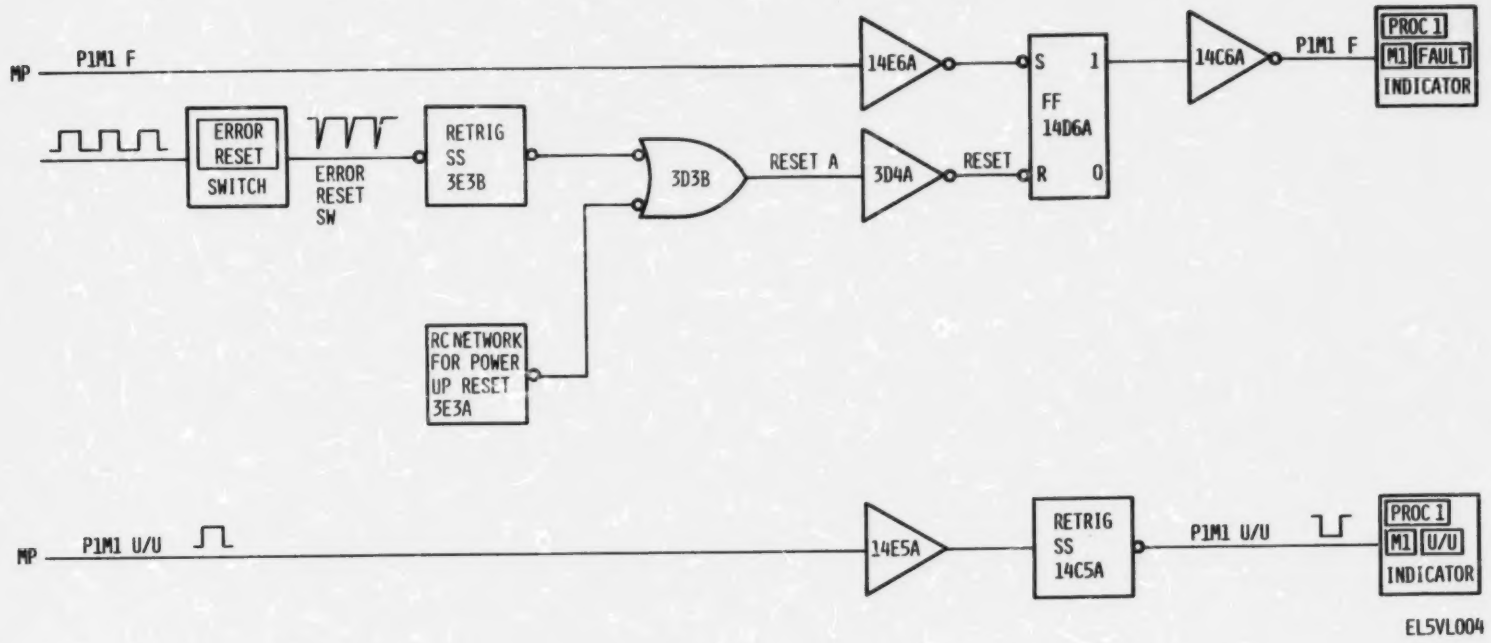

Figure 4-5. Typical Fault Indicator Panel Logic, Block Diagram.

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NOTE

The failure and unit-available input levels from the message processor (MP) are −0.5 V dc for a low and +0.5 V dc for a high.

(1) When a processor 1, memory 1, failure indication (P1M1F high) is received from the MP, FF 14D6A is set. The 1 output of FF 14D6A goes high, turning on the PROC 1 M1 FAULT indicator. The indicator remains on until FF 14D6A is reset. Initial contact with the ERROR RESET switch causes a series of negative pulses (ERROR RESET SW) which trigger single-shot 3E3B, resulting in a reset of FF 14D6A. FF 14D6A is also reset during a power-up sequence by a resistive-capacitive network (3E3A) which generates a low to gate 3D3B.

NOTE

The power up sequence and the ERROR RESET switch will reset all fault indicator panel fault indicators.

(2) When a unit-unavailable indication (P1M1 U/U high) is received from the MP, SS 14C5A is fired. The low output of the single-shot turns on the PROC 1 M1 U/U indicator. The P1M1 U/U high input can be of very short duration and would not be visible on the LED indicator; therefore, the single-shot is used to extend the time duration of each unit-unavailable signal, allowing visual detection.

4-3. Processor Maintenance Circuits

The processor maintenance circuits (fig. 4-1 and 4-6) consist of the processor panels, and the processor logic is used to display various data and control signal outputs of a 102 processor and to switch control and data signals to a 102 processor. Indicator drivers in the processor logic are used to operate the indicators on the processor panel. Switch output drivers amplify some of the switch signals sent to the 102 processor from various switches on the processor panel.

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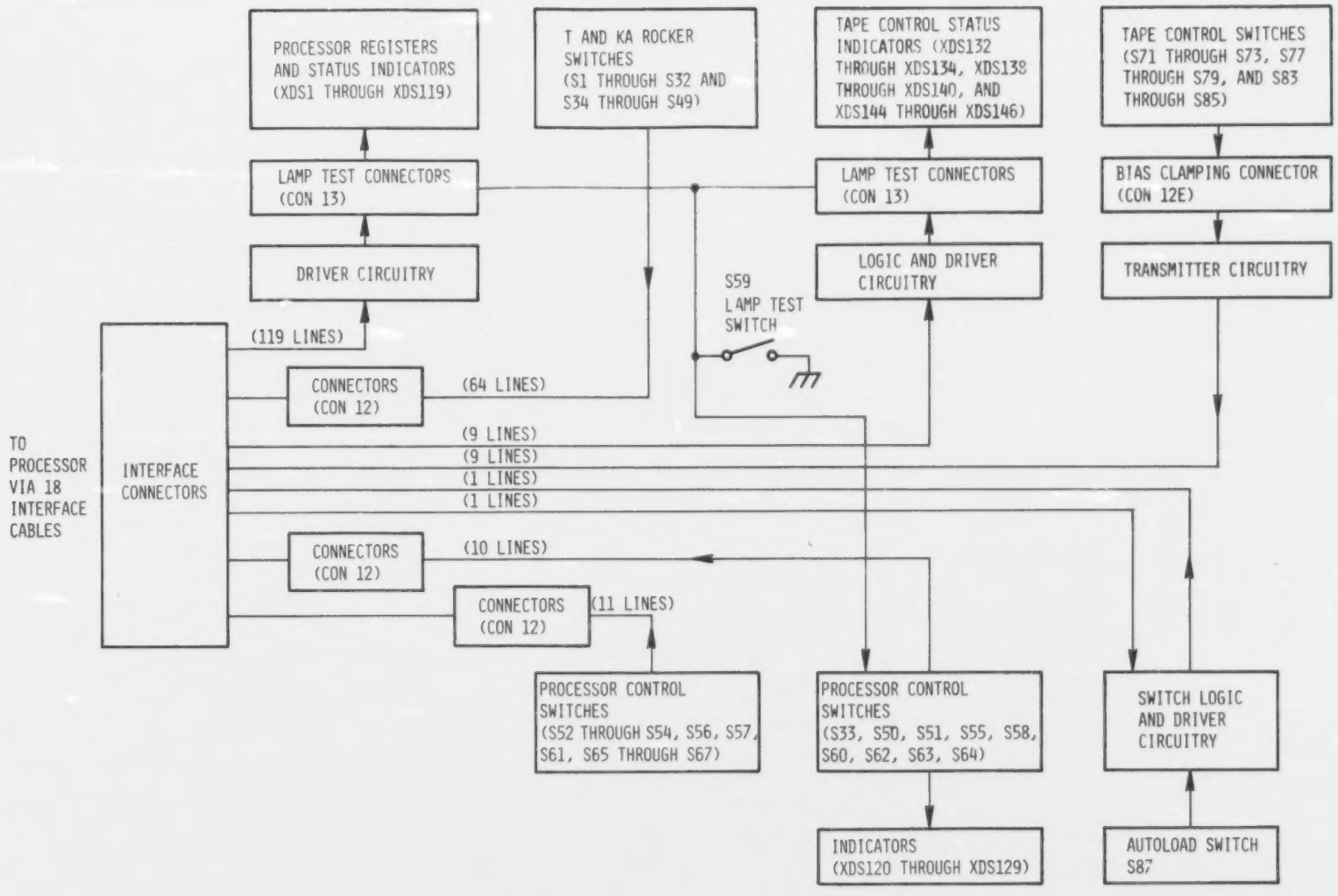
PROCESSOR REGISTERS AND STATUS INDICATORS (XDS1 THROUGH XDS119)
T AND KA ROCKER SWITCHES (S1 THROUGH S32 AND S34 THROUGH S49)
TAPE CONTROL STATUS INDICATORS (XDS132 THROUGH XDS134, XDS138 THROUGH XDS140, AND XDS144 THROUGH XDS146)
TAPE CONTROL SWITCHES (S71 THROUGH S73, S77 THROUGH S79, AND S83 THROUGH S85)
LAMP TEST CONNECTORS (CON 13)
LAMP TEST CONNECTORS (CON 13)
BIAS CLAMPING CONNECTOR (CON 12E)
DRIVER CIRCUITRY
LOGIC AND DRIVER CIRCUITRY
TRANSMITTER CIRCUITRY
S59 LAMP TEST SWITCH
(119 LINES)
CONNECTORS (CON 12)
(64 LINES)
TO PROCESSOR VIA 18 INTERFACE CABLES
INTERFACE CONNECTORS
(9 LINES)
(9 LINES)
(1 LINES)
(1 LINES)
CONNECTORS (CON 12)
(10 LINES)
CONNECTORS (CON 12)
(11 LINES)
PROCESSOR CONTROL SWITCHES (S52 THROUGH S54, S56, S57, S61, S65 THROUGH S67)
PROCESSOR CONTROL SWITCHES (S33, S50, S51, S55, S58, S60, S62, S63, S64)
SWITCH LOGIC AND DRIVER CIRCUITRY
INDICATORS (XDS120 THROUGH XDS129)
AUTOLOAD SWITCH S87
EL5VL013

Figure 4-6. SSCC Processor Panel (Typical), Functional Block Diagram.

a. Processor Indicator Functions. All indicators in the upper four rows of indicators on the processor panel are operated by signals from the 102 processor. The individual indicator signals are routed through lamp drivers shown on drawing 9L08948, sheets 41 through 48. The significance of the individual indicators is given in chapter 3.

b. Processor Switch and Switch-Indicator Functions (fig. FO-5 and FO-6).

(1) All switches on a processor panel (except TAPE and LAMP TEST) are used to provide contact closures for dc voltages to a 102 processor. The functional significance of the individual switch operations is given in chapter 3.

(2) The normally-open and normally-closed contacts of each K rocker switch are connected to −5.6 V dc and +5.1 V dc (generated at E2 and E4 on figure FO-6, sheet 7), while the common contact is used as the output to the interface. The normally-open and normally-closed contacts of each T rocker switch are connected to +5.1 V dc and ground, while the common contact is used as the output to the interface. For KA rocker switches, strapping is performed to a second set of contacts so that two outputs are available for each switch. Typical switch connections for the T and KA rocker switches are shown in figure FO-5 and figure FO-6, sheets 5 and 6. The outputs from all rocker switches are applied through connector boards CON 12C and CON 12G to interface connectors on the D and E levels.

c. Tape Status Indicators (fig. FO-3).

(1) Signals related to the status of up to three tape controllers are transmitted from a 102 processor unit to each processor panel via the signal and data interface cables. The indicators are located within the tape control switches on the panel although there is no direct relationship between the two. The indicator circuits for the tape controllers are identical and the following description applies to each circuit.

(2) The indicator signals enter a processor panel from a 102 processor at interface connector C41. Each signal is fed to a driver network consisting of a IRRA logic receiver and a 1MLDA lamp driver. 1GB inverters are connected to the RUN indicator driver so that the RUN indicator does not illuminate while the associated HALT or FAULT indicator is illuminated. The output of each lamp driver is applied to its associated lamp in a manner identical to that described for the processor registers and status indicators in b(2) above, through connector board CON 13.

d. Tape Control Switches (fig. FO-3).

(1) Momentary-action switches are provided on the panel to control the operation (clear, halt, continue) of tape controllers associated with the connected processor. Signals generated by these switch circuits are transmitted to the processor unit via the signal and data interface cables. The switch circuits are identical and the following discussion applies to each circuit.

(2) The normally-closed and normally-open contacts of each switch are connected to +5.1 V dc and −5.6 V dc, while the common contact is used as the output (fig. FO-6, sheet 4). The output from each switch (+5.1 V dc or −5.6 V dc) is applied to a bias clamping circuit as shown in figure 4-7. This circuit clamps the signal input level to a logic transmitter at −5.6 ±0.5 V dc or +4.0 ±0.5 V dc as determined by the voltage divider circuit between the selected source voltage and −5.6 V dc. The output of the logic transmitters is applied to the interface connector at C44.

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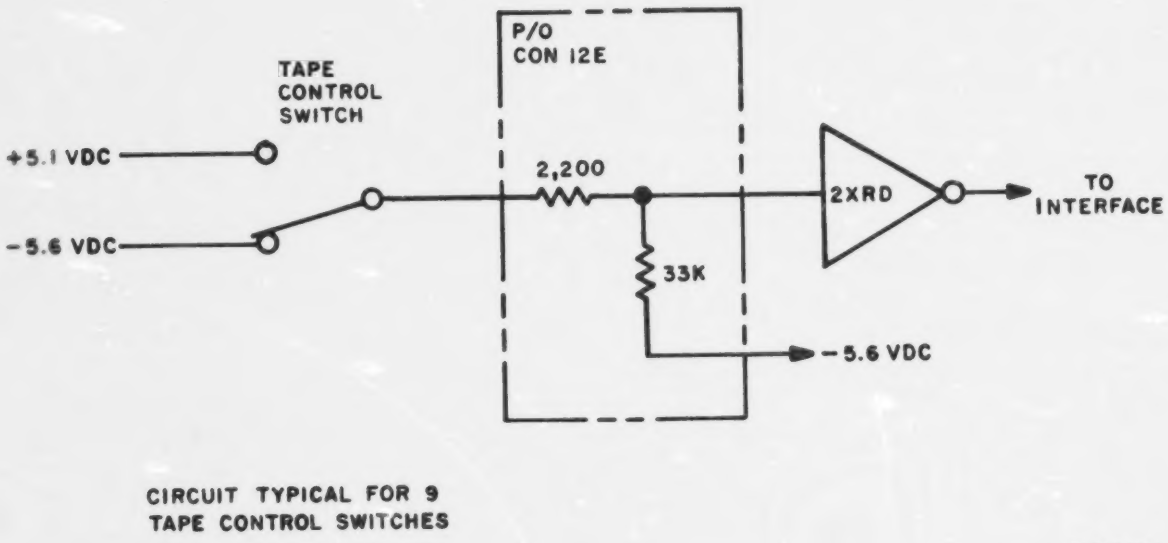

Figure 4-7. SSCC Processor Panel, Tape Control Switch Bias Clamping Circuit.

e. Processor Control Switches and Switch/Indicators (fig. FO-3).

(1) These switches and indicators consist of the FAULT ACTION and OPERATE rocker switches and all of the momentary-action switches and alternate-action switch/indicators on the lower portion of the console panel (with the exception of the LAMP TEST switch). All of these switches and switch/indicators operate in basically the same manner with only slight variations for certain circuits. The following discussion will cover all circuits with variations for certain circuits noted as required.

(2) As shown in figure FO-6, sheet 3, all switch common contacts (except PROC STOP, IOC STOP, and STOP ON STORE ONLY) are connected to +5.1 V dc only, with their outputs being +5.1 V dc or 0.0 V dc. The +5.1 V dc operating voltage to the DISPLAY, STORE, AUTO LOAD, LOAD PA, CLEAR, and SET SCANNER momentary-action switches is provided through the common and normally-closed contacts of the RUN switch to prohibit use of these switches when the RUN switch is active. All switches have one output line with the exception of the RUN alternate-action switch and the FAULT ACTION and OPERATE rocker switches. The RUN switch has an output taken from its normally-closed contact in addition to its normally-open contact. Each of the rocker switches is inactive when in a center position and active when in an up or down position. This necessitates two outputs from these switches. The switch outputs (+5.1 V dc or 0.0 V dc) are applied through connector boards CON 12C and CON 12G to interface connectors on the B, D, and E levels.

(3) As shown in figure FO-6, sheet 3, each of the alternate-action switches has associated indicators located within the pushbutton which illuminate when the switch is in the active state. One side of each indicator is connected to −27 V dc. The other side is connected, through a dropping resistor, to a common contact of the alternate-action switch. The normally-open contact of this set of contacts is returned to ground. When the alternative-action switch is in its active state, current flows through these switch contacts and the dropping resistor to light the indicator.

4-4. Lamp Test Circuit Description

a. The LAMP TEST switch provides for checking for faulty indicator lamps on the panel. Logic circuitry is not tested as the lamp test circuit is completely independent of the normal indicator lamp energizing circuit. All 102 processor content and status indicators and tape status indicators are lighted in one manner while all alternate-action switch indicators are lighted in a second manner. The following discussion covers each method of lighting an indicator during the lamp test.

b. Basically, the lamp test circuit operates by grounding one side of every panel indicator. As previously mentioned, this is accomplished in two ways. For all of the alternate-action switch/indicators,

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lamp ground is applied from E6 of the power supply through the normally-open contacts of S59 (fig. 4-8) to contact 4 of all of the alternate-action switches. With these switches in their normal inactive position, the ground is applied through the dropping resistor to the indicator, thereby causing it to light.

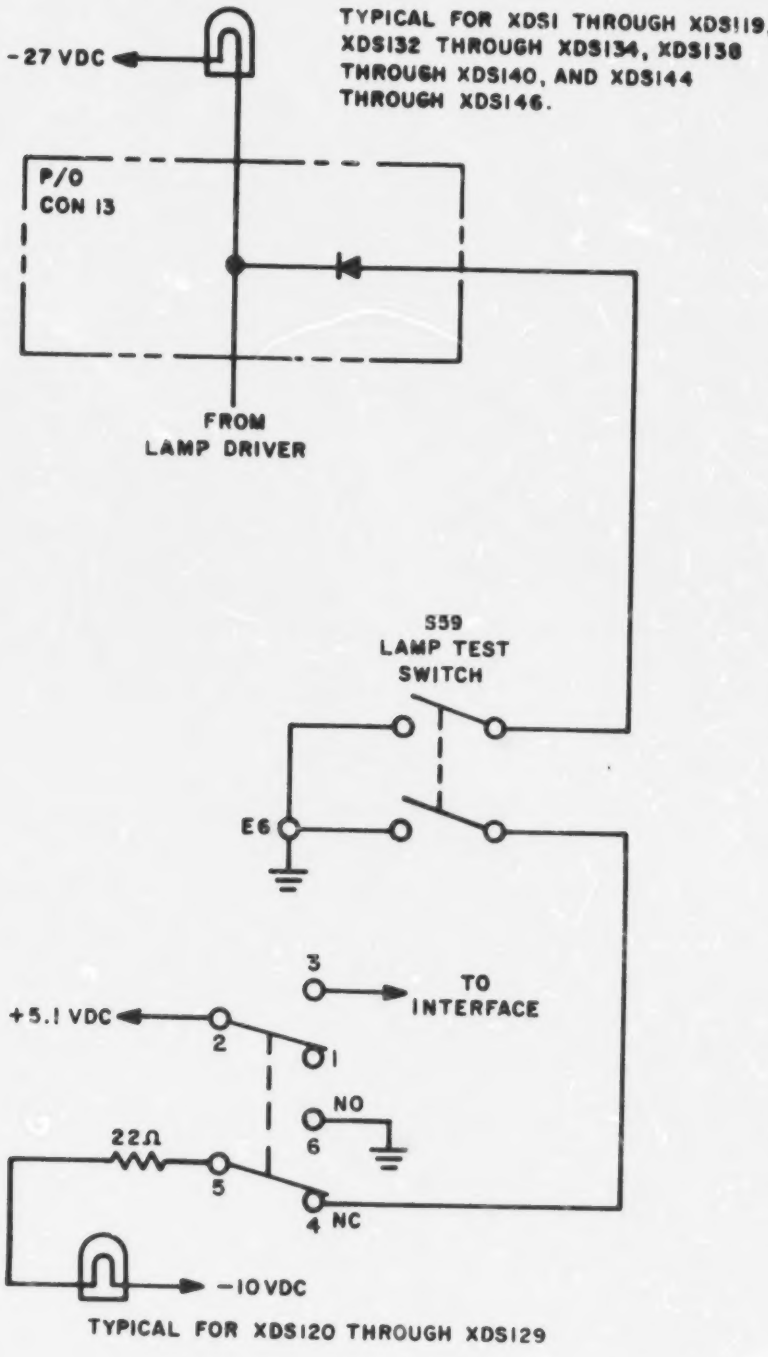

Figure 4-8. SSCC Processor Panel, Typical Lamp Test Circuit.

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c. For all other indicator lamps on the console panel, ground is applied from E6 of the power supply, through shorted plug-in cards to normally-open contacts of LAMP TEST switch S59. With the switch activated, this ground is applied to pins 1 and 30 of the diode lamp test connector cards at A41, A42, A43, A44, and A60. The 28 diodes on each card are thus forward biased (ground on anode, −27 V dc on cathode), allowing each of the indicators to light.

4-5. SSCC Power Supplies and Power Controller

The power supplies of the SSCC are shown in figure 4-9. The power supply controller routes 120 V ac, 60 Hz primary power to each of the power supplies. The power supply controller is described in TM 11-5895-552-15/1, Tm 11-5895-552/2, and TM 11-5895-552-15/3.

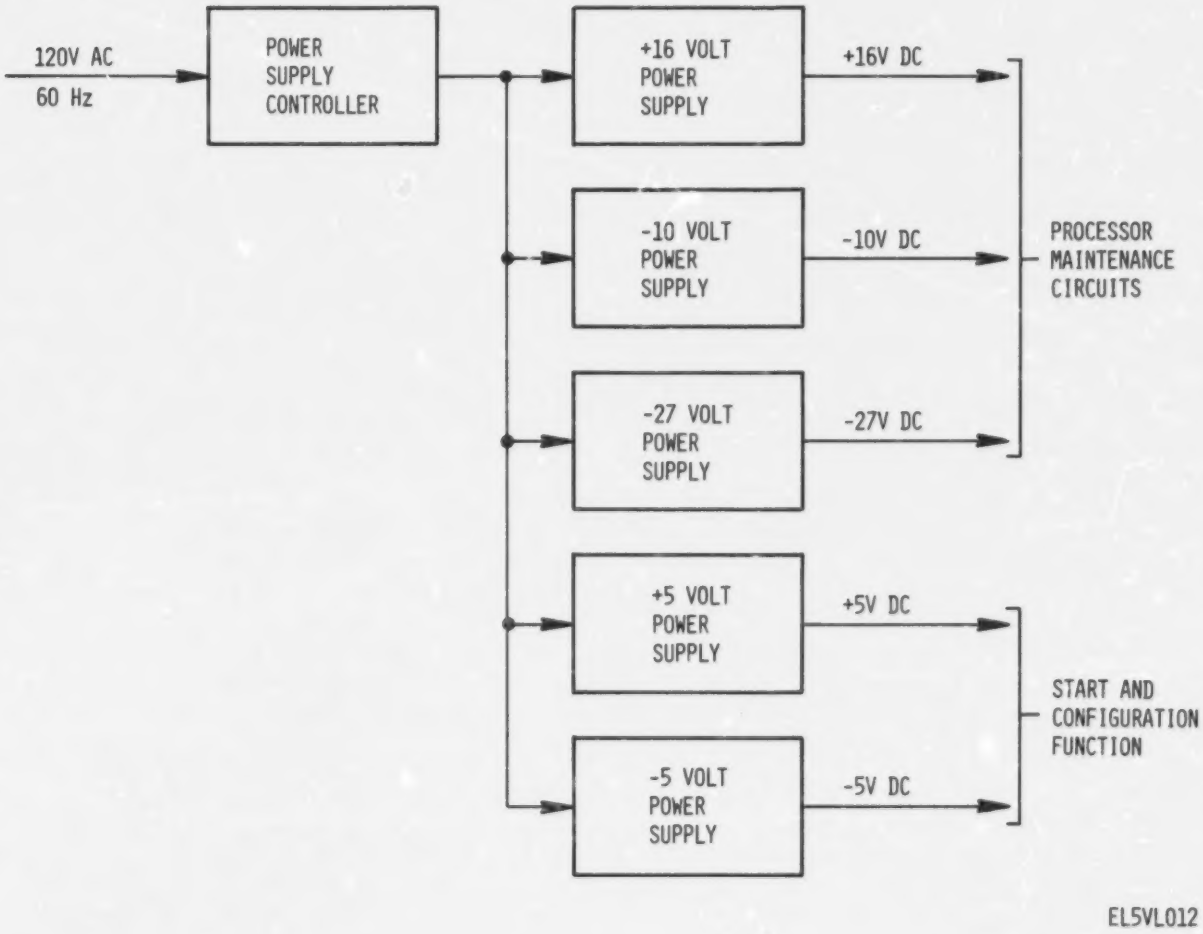

Figure 4-9. SSCC Power Supply Circuits, Block Diagram.

a. +16 V DC, −10 V DC, and −27 V DC Power Supply Theory of Operation. The theory of operation for the +16 V dc, −10 V dc, and −27 V dc power supplies is described in TM 11-5895-552-15/1, TM 11-5895-552-15/2, and TM 11-5895-552-15/3.

b. +5 V DC and −5 V DC Power Supply Theory of Operation.

(1) *+5 V dc power supply, PS2, model LCS-CC-5-OV.* (Refer to block diagram, figure 4-10 and schematic diagram, figure FO-8.)

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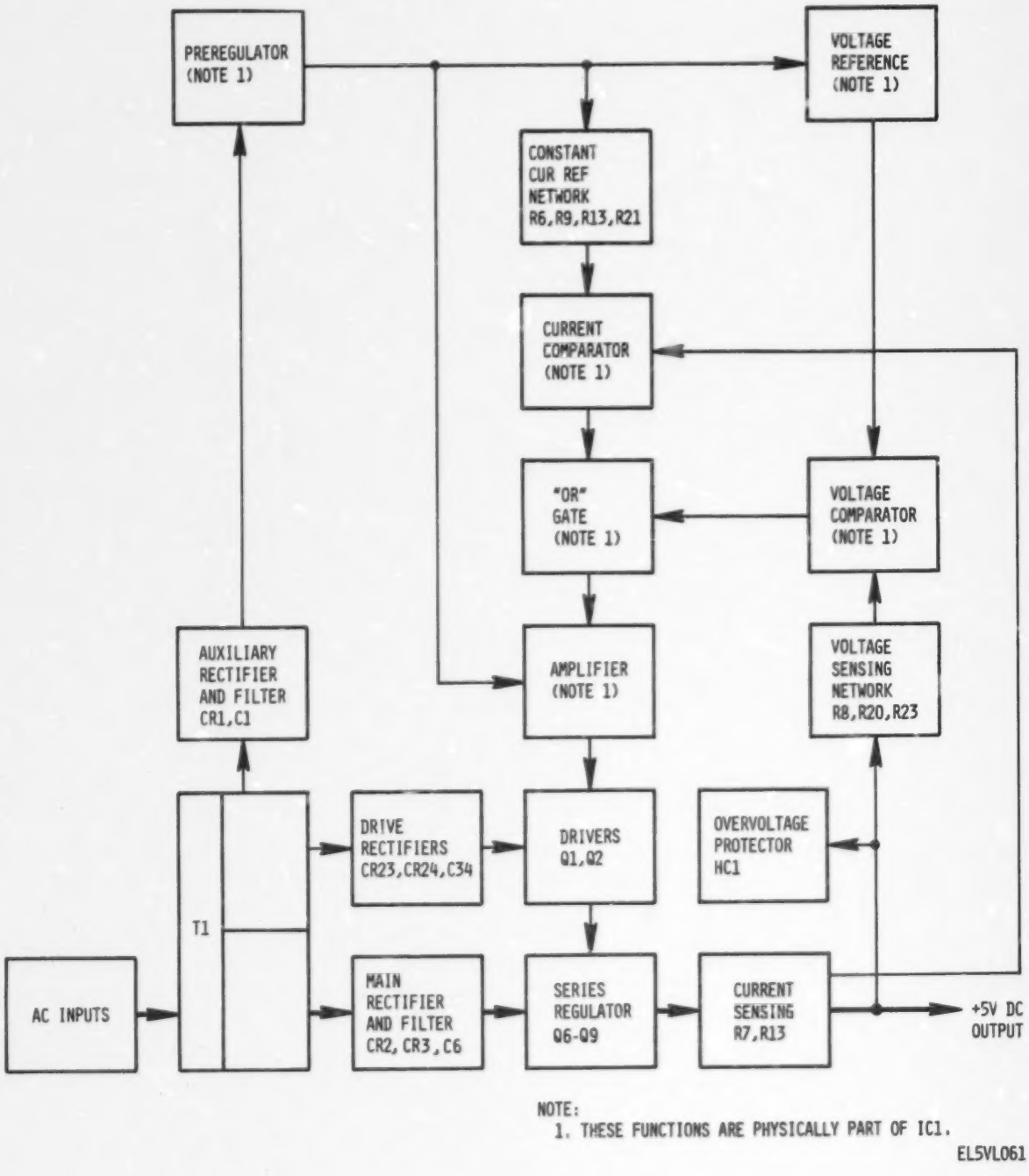

Figure 4-10. +5 V DC Power Supply, PS2, Block Diagram.

(a) Single-phase 115 V ac input power is applied to transformer T1 via the input circuit. The input circuit contains a thermostat (S1) which protects the power supply by opening the 115 V ac input line in the event of an overheat condition. The main rectifier (a full wave rectifier comprised of CR2 and CR3) provides dc power which is filtered by C6 and then regulated by series regulators Q6 through Q9. Half-wave auxiliary rectified CR1 provides dc power which is filtered by C1 and routed to the preregulator function of integrated circuit IC1. The reference elements, powered by the preregulator, provide reference voltages for the current comparator and the voltage comparator. Full-wave drive rectifier CR23

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4/9

and CR24 provides dc power, filtered by C34, for drivers Q1 and Q2.

(b) Constant-voltage output is maintained by sensing voltage changes in the load (IC1-6) which are applied to one input of the voltage comparator. The second input to the comparator is a reference voltage which is developed by a constant current of 1 mA through voltage sensing network R8, R20, and R23. The position of potentiometer R8 will determine the reference voltage (IC1-8). The voltage comparator compares the output voltage change with the reference voltage and generates an error signal. The error signal is amplified and output (IC1-5) to drivers Q1 and Q2. The current amplified output of Q1 and Q2 controls the voltage across series regulators Q6 through Q9, which function as the active regulating elements in the power supply.

(c) Current-limit operation is accomplished by sensing current changes in the load (IC1-11) which are applied to one input of the current comparator. This input is determined by the position of potentiometer R13, which senses the current through current-sensing resistor R25. The second (reference) input IC1-10) to the current comparator is determined by constant-current reference network R6, R9, R13, and R21. When the load current increases above the rated current value (determined by the value of R6, R9, R21, R25, and the setting of R13), the error signal from the amplifier (IC1-5) reduces the current through drivers Q1 and Q2, reducing the base current to series regulators Q6 through Q9. This results in an increase of voltage across Q6 through Q9 and a decrease of the output voltage, effectively limiting the output current to a safe level. If operating conditions reach a short circuit, the output voltage decreases to 0 and the current remains at the safe-current-limit value.

(d) Overvoltage protection is provided by HC1. If the output voltage increases above the overvoltage limit (+6.4 V dc to +6.8 V dc), HC1 fires, causing the power supply output voltage to drop.

(2) *−5 V dc power supply, PS1, model LCS-B-5-OV.* (Refer to block diagram, figure 4-11; and schematic diagram, figure FO-7, sheet 1 for serial number prefixes C and D, and sheet 2 for serial number prefixes from F on.)

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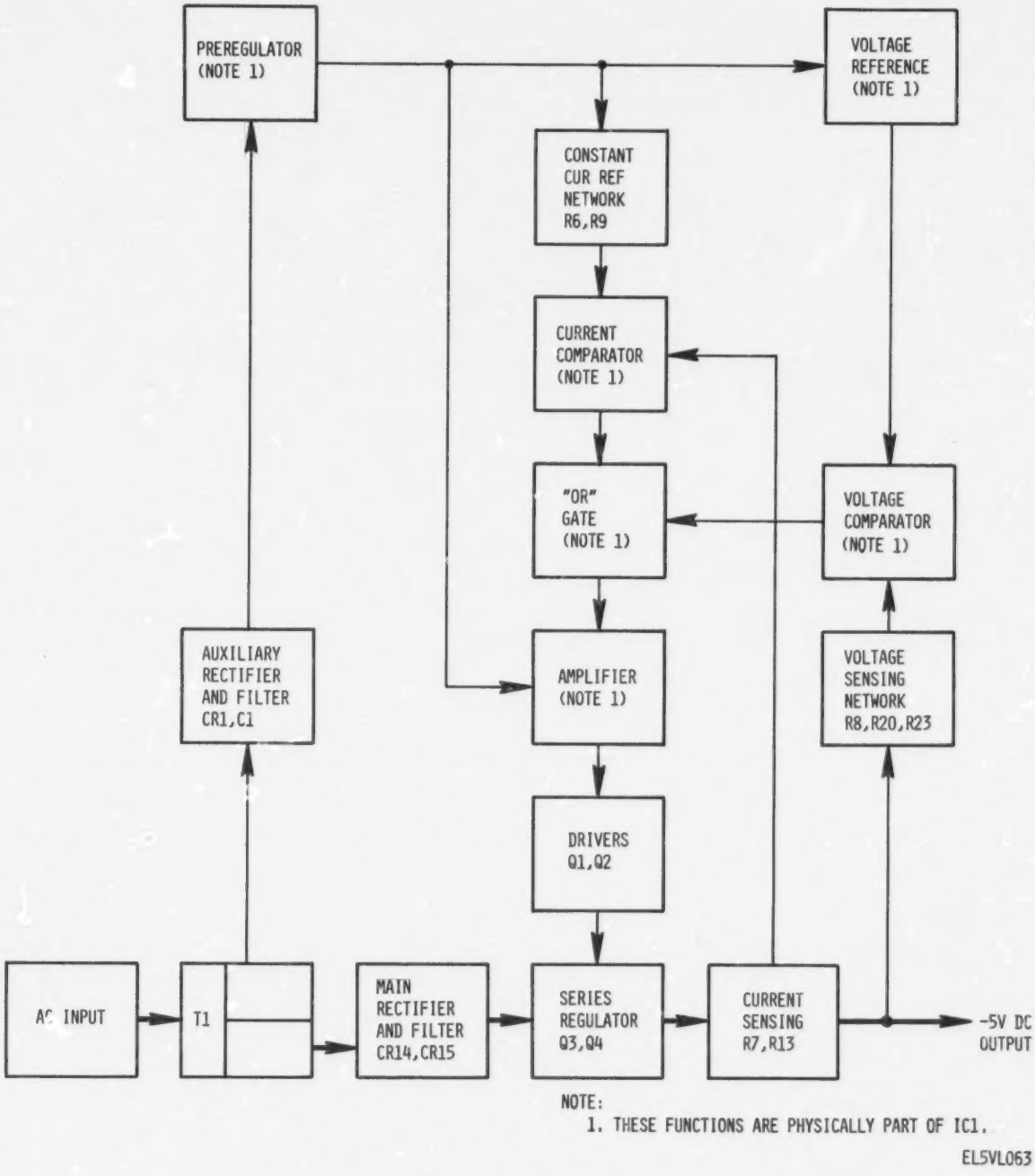

Figure 4-11. −5 V DC Power Supply, PS1, Block Diagram.

(a) Single-phase 115 V ac input power is applied to transformer T1 via the input circuit. The input circuit contains a thermostat (S1) which protects the power supply by opening the 115 V ac input line in the event of an overheat condition. The main rectifier (a full wave rectifier comprised by CR14 and CR15) provides dc power which is filtered by C3 and C6 and then regulated by series regulator Q3 and Q4. Half-wave auxiliary rectifier CR1 provides dc power which is filtered by C1 and routed to the preregulator function of integrated circuit IC1. The reference elements, powered by the preregulator, provide refer-

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ence voltages for the current comparator and the voltage comparator.

(b) Constant-voltage output is maintained by sensing voltage changes in the load (IC1-6) which are applied to one input of the voltage comparator. The second input to the comparator is a reference voltage which is developed by a constant current of 1 mA through voltage sensing network R8, R20 and R23. The position of potentiometer R8 will determine the reference voltage (IC1-8). The voltage comparator compares the output voltage change with the reference voltage and generates an error signal. The error signal is amplified and output (IC1-5) to drivers Q1 and Q2. The current amplified output of Q1 and Q2 controls the voltage across series regulators Q3 and Q4, which function as the active regulating elements in the power supply.

(c) Current-limit operation is accomplished by sensing current changes in the load (IC1-11) which are applied to one input of the current comparator. This input is determined by the position of potentiometer R13, which senses the current through current-sensing resistor R7. The second (reference) input (IC1-10) to the current comparator is determined by constant-current reference network R6, R9, R13, and R21. When the load current increases above the rated current value (determined by the value of R6, R9, R21, and the setting of R13) the error signal from the amplifier (IC1-5) reduces the current through drivers Q1 and Q2, reducing the base current to series regulators Q3 and Q4. This results in an increase of voltage across Q3 and Q4 and a decrease of the output voltage, effectively limiting the output current to a safe level. If operating conditions reach a short circuit, the output voltage decreases to 0 and the current remains at the safe-current-limit value.

4-6. DC Power Distribution

a. Processor Panel Power Distribution. All dc power distribution to the processor panel logic pans is accomplished through dc bus lines located throughout the SSCC. The arrangement of these bus lines is shown on sheet 6 of drawing 590-1192 of TM 11-5895-747-15. Figure 4-12, sheet 1 illustrates how the dc voltages from the bus lines service the logic pans within the processor panels. For detail bus designation, refer to drawing 590-1177 of TM 11-5895-747-15, in conjunction with figure 4-12, sheet 1. Due to the fact that voltage distribution is functionally the same within the logic cards mounted throughout the bays, the functional description given below is applicable to each logic pan within the SSCC.

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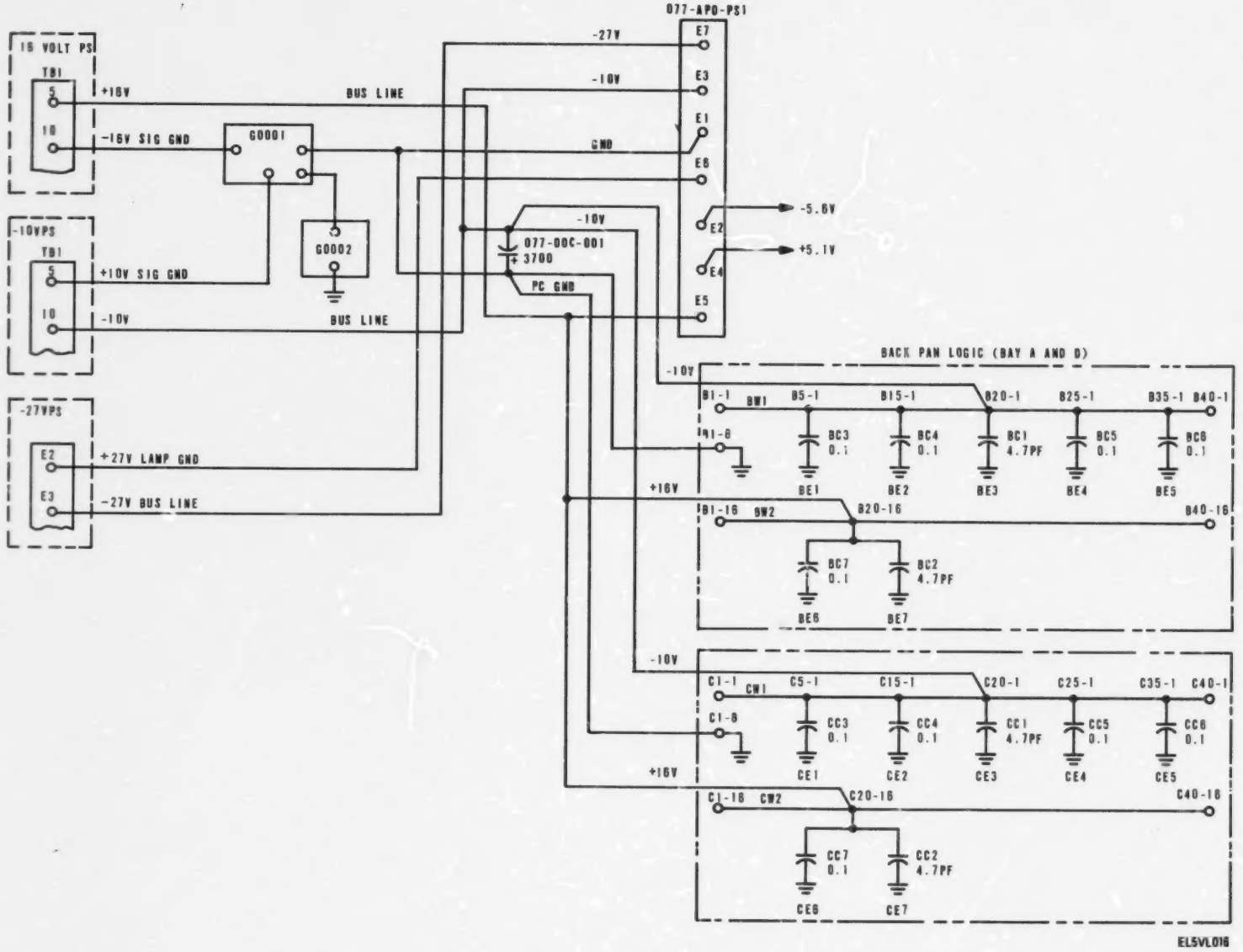

Figure 4-12(1). DC Power Distribution, Schematic Diagram (Sheet 1 of 2).

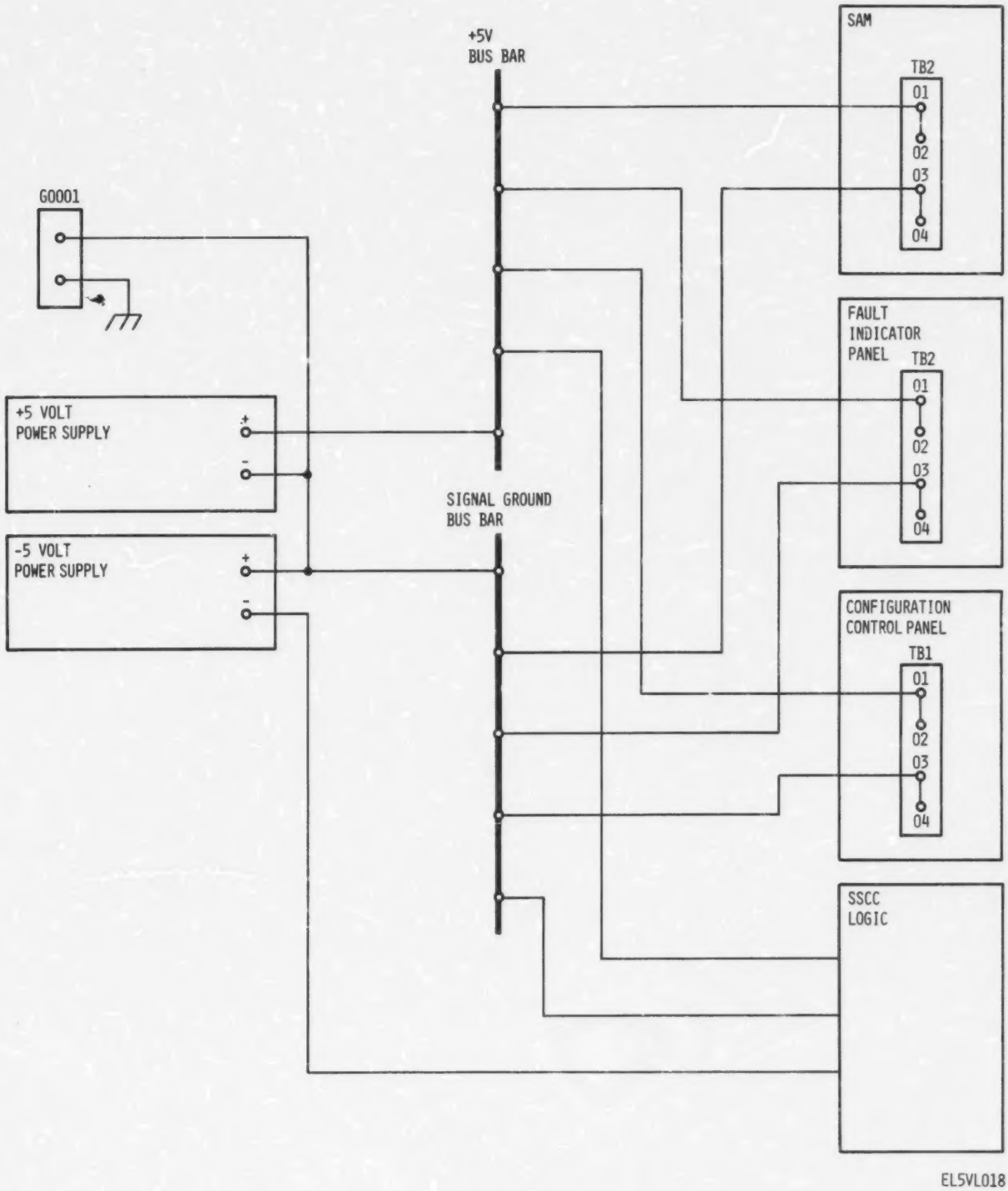

Figure 4-12(2). DC Power Distribution, Schematic Diagram (Sheet 2 of 2).

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(1) As shown in figure 4-12, sheet 1, −27 V dc is supplied from the −27 V dc bus to standoff E7 on power supply 077-APO-PS1 (fig. FO-6, sheet 7). Standoff E7 supplies −27 V dc to all indicating lamps on the SSCC panels. The E6 standoff provides lamp ground for the lamp test switches.

(2) As shown in figure 4-12, sheet 1, −10 V dc is supplied to pin 1 of every back pan logic receptacle on the B and C levels. Five capacitors are connected between the −10 V dc line and ground on each level to provide additional filtering. Ground for the logic cards is provided at terminal 8 of each terminal board. The −10 V dc is also supplied to standoff E3 on power supply 077-APO-PS1, as shown in figure FO-6, sheet 7. This voltage is required for generating −5.6 V dc control switches, as described in paragraph 4-3.

(3) The +16 V dc is supplied to pin 16 of every back pan logic receptacle. Two capacitors are connected between the line and ground on each level to provide filtering of the +16 V dc potential. The +16 V dc is also connected to standoff E5 of the power supply for use in generating +5.1 V dc for control switches, as described in paragraph 4-3.

b. SSCC Logic Power Distribution. Dc power distribution is shown on figure 4-12, sheet 2. The +5 V dc output of the +5 V dc power supply is tied to a bus bar which routes it to the SAM panel, the fault indicator panel, the configuration control panel, and the SSCC logic board. Signal ground is also tied to a bus bar and routed to the same units. The −5 V dc from the −5 V dc power supply is routed directly to the SSCC logic board.

Section II. SSCC LOGIC BASIC MODULES

4-7. General

Logic circuits used in the SSCC logic are contained in plug-in integrated circuit modules. All modules are sealed assemblies and are nonrepairable. Repairs are effected by replacing the defective module.

a. Logic Levels. Logic levels within the SSCC logic are referred to as high and low. Unless otherwise specified, high levels are between +2.4 and +5.0 V dc and low levels are between 0.0 and +0.6 V dc.

b. Pin Arrangements. The basic modules are standard 14- and 16-pin dual in-line modules (fig. 4-13). All connectors for these modules have 16 pins regardless of whether the module is a 14- or 16-pin package. Where the module has 14 pins, pins 8 and 9 of the connector are not used. The basic module descriptions and illustrations in this section refer to module pins and not to connector pins. However, the SSCC logic theory description and illustrations in chapter 4, section I and the detailed logic diagrams in TM 11-5895-404-15/2 refer to connector pins, not module pins. Figure 4-14 provides a cross-reference between module- and connector-pin arrangements.

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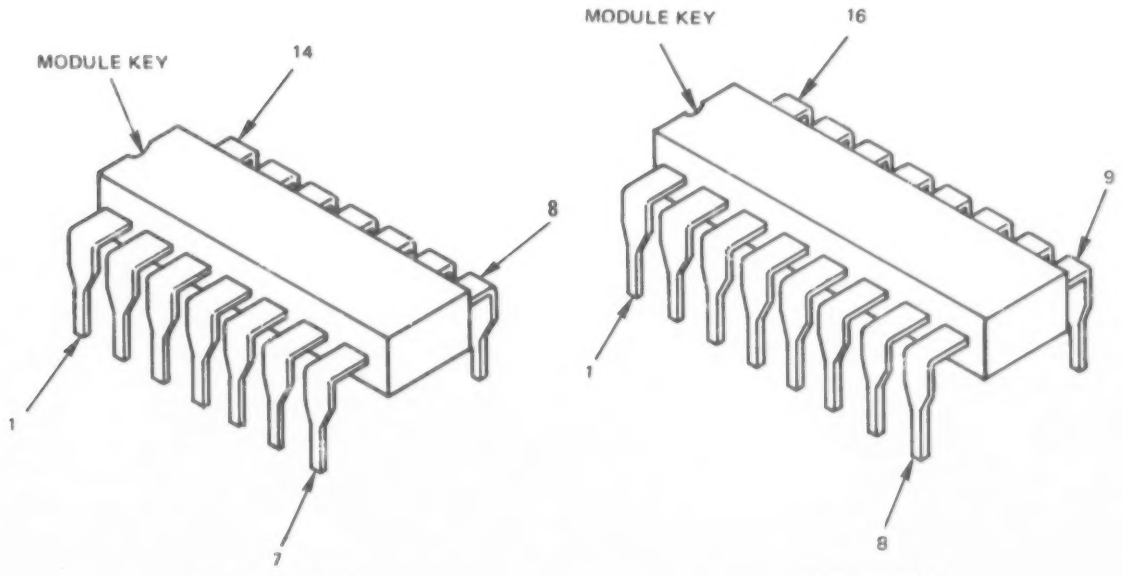

NOTES:

1. SOME MODULES HAVE A KEY AT BOTH ENDS AND A DOT. THE DOT TAKES PRECEDENCE IN IDENTIFYING PIN 1.
2. WHEN NO DOT APPEARS ON THE MODULE, PIN 1 IS LOCATED TO THE LEFT OF THE KEY.

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Figure 4-13. Standard Dual In-Line Modules.

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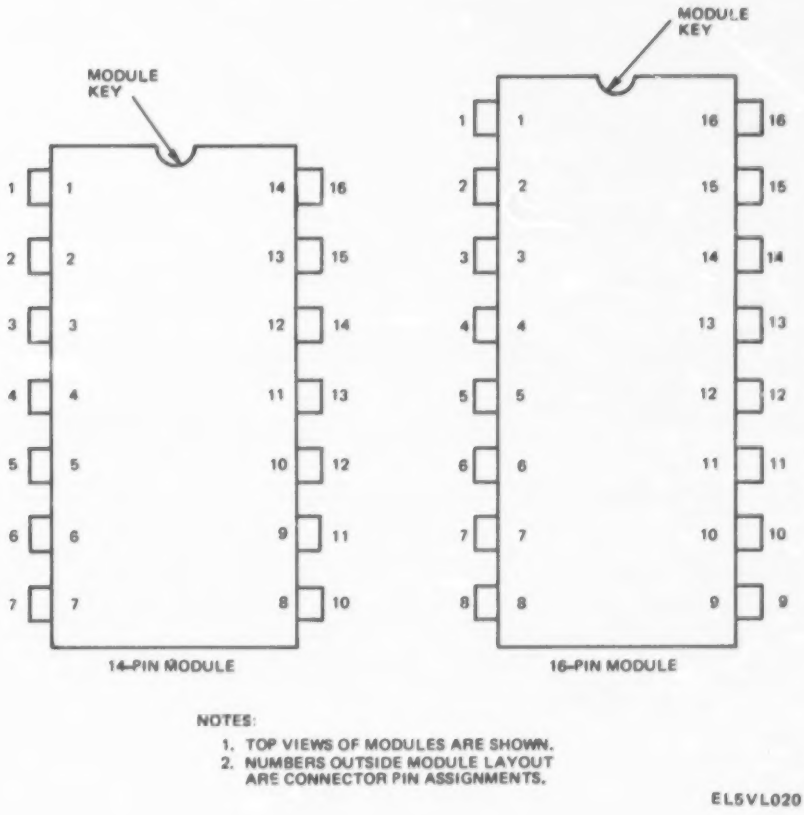

Figure 4-14. Module-to-Connector-Pin-Number Cross Reference.

4-8. Module Descriptions

The following paragraphs describe each type of module used in the SSCC logic. The modules are listed in alphanumeric order by mnemonic identifier to facilitate referencing. Manufacturer's part numbers are shown in parentheses. Illustrations show the module pin designations assigned by the manufacturer.

a. Capacitor Pack CAP102 (9363C102XOSR) (fig. 4-15). The CAP102 module contains eight 1000 pF capacitors.

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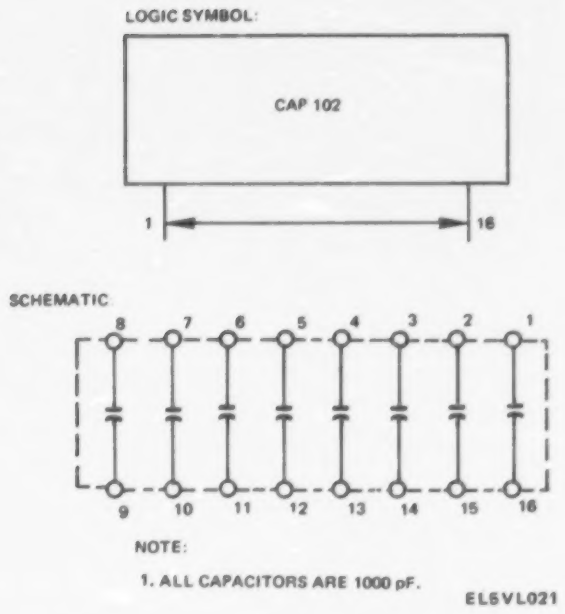

Figure 4-15. Capacitor Pack CAP102 (936C102XOSR), Logic Symbol and Schematic Diagram.

b. Capacitor Pack CAP104 (936C104XOSR) (fig. 4-16). The CAP104 module contains eight 0.1 μF capacitors.

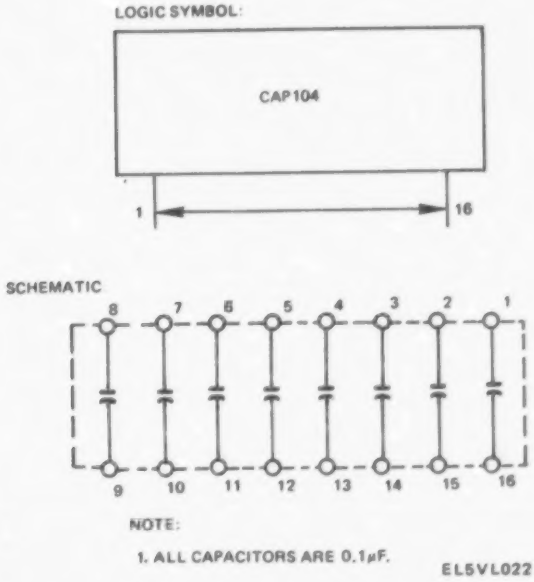

Figure 4-16. Capcitor Pack CAP104 (936C104XOSR), Logic Symboi and Schematic Diagram.

c. Capacitor Pack CAP332 (936C332XOSR) (fig. 4-17). The CAP332 module contains eight 3300 pF capacitors.

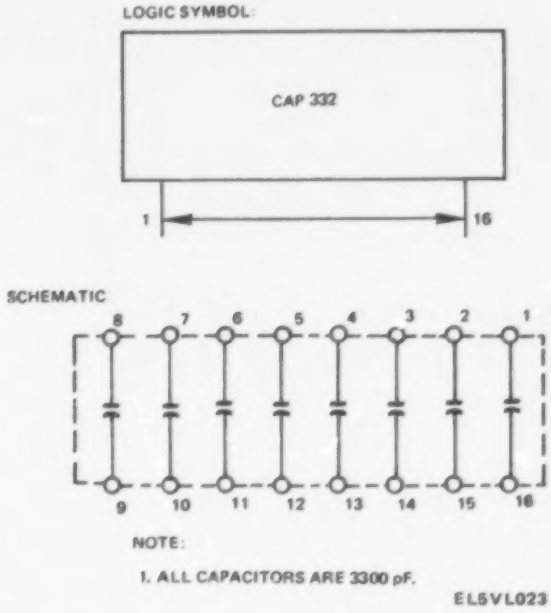

Figure 4-17. Capacitor Pack CAP 332 (936C332XOSR), Logic Symbol and Schematic Diagram.

d. Capacitor Pack CAP471 (936C471XOSR) (fig. 4-18). The CAP471 module contains eight 470 pF capacitors.

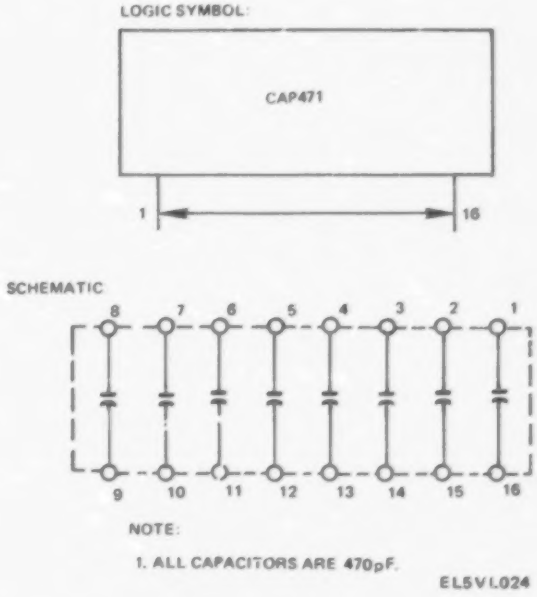

Figure 4-18. Capacitor Pack CAP471 (936C471XOSR), Logic Symbol and Schematic Diagram.

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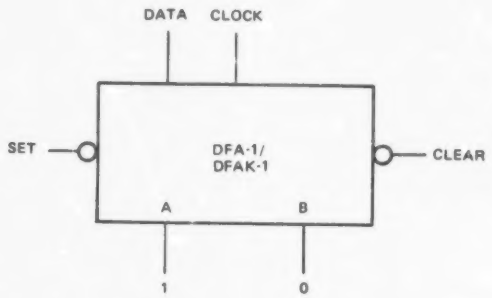
e. Dual D-Type Flip-Flops DFA-1, DFAK-1, (7474, 74LS74) (fig. 4-19). The DFA-1 and DFAK-1 modules contain two positive-edge-triggered flip-flops with individual set and clear inputs. Each flip-flop has complementary outputs. Application of a low to the set input sets the 1 output to a high level and the 0 output to a low level. Application of a low to the clear input sets the 1 output to a low level and the 0 output to a high level. With the clear and set inputs high, data applied to the data input is transferred to the 1 output on the positive edge of the clock pulse.

f. Line Driver LDA (75110) (fig. 4-20). The line driver module contains two independent channels with a common voltage supply and ground terminals. The driver circuits provide a constant output current that is switched to either of two output terminals by appropriate logic levels at the input terminals. The truth table on figure 4-20 provides LDA module outputs for the input-level combinations.



VCC – PIN 14
GND – PIN 7

PIN ARRANGEMENT

CIRCUIT NO	PIN NO					
	DATA	CLOCK	SET	CLEAR	1	0
1	2	3	4	1	5	6
2	12	11	10	13	9	8

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Figure 4-19. Dual D-Type Flip-Flops DFA-1, DFAK-1 (7474, 74LS74), Logic Symbol and Pin Arrangement.

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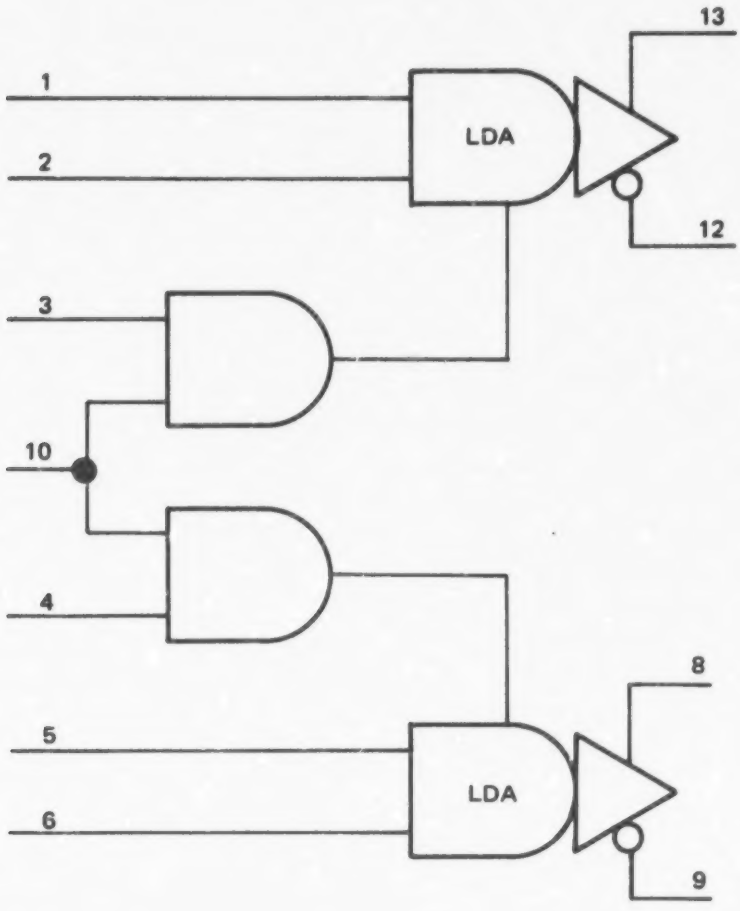

VCC – PIN 14
GND – PIN 7
NC – PIN 11

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
1	2	3	10	13	12
X	X	L	X	H	h
X	X	X	L	H	H
L	X	H	H	L	H
X	L	H	H	L	H
H	H	H	H	H	L

H = HIGH LEVEL
L = LOW LEVEL
X = HIGH OR LOW LEVEL

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Figure 4-20. Line Driver LDA (75110), Logic Symbol and Pin Arrangement.

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60.

g. Line Receiver LRA (75107AJ and 75107AN) (fig. 4-21). Each LRA module contains two identical circuits which function as level converters and serve as the line interface receivers between the computer or external devices and the memory control assembly. Each line receiver consists of a differential amplifier and a 2-input gate. Logic-level conversion is controlled by a reference voltage input (pins 1 and 14) to produce TTL output levels (+5 V dc and 0 V dc) required by the memory control assembly logic. Data inversion is accomplished by connecting the data inputs to the inverting inputs of the differential amplifier.

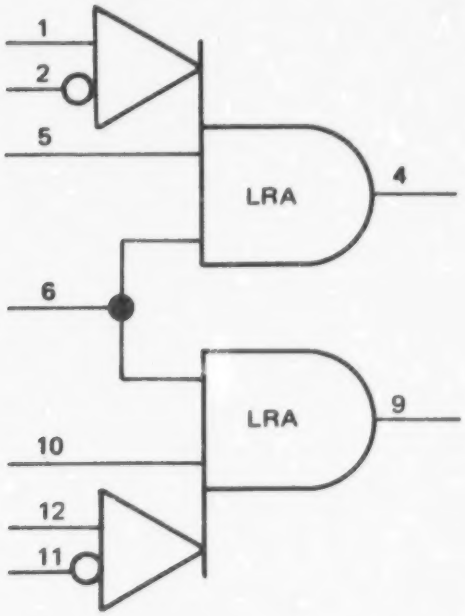

Figure 4-21. Line Receivers LRA (75107AJ and 75107AN), Logic Symbol and Pin Arrangement.

h. Dual Retriggerable Monostable Multivibrator MVC-1 (74123J) (fig. 4-22). The MVC-1 module contains two retriggerable multivibrators. The multivibrators feature dc triggering from gated low-level-active (A) and high-level-active (B) inputs and also provide overriding direct clear inputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independent of the timing components, R and C.

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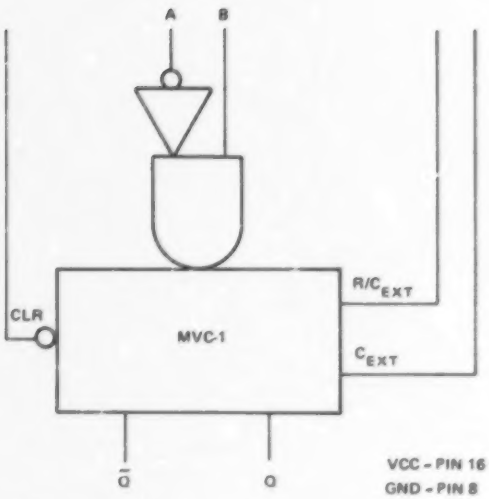

PIN ARRANGEMENT

CIRCUIT NO	A	B	CLR	Q̄	Q	C_{EXT}	R/C_{EXT}
1	1	2	3	4	13	14	15
2	9	10	11	12	5	6	7

TRUTH TABLE

INPUTS			OUTPUTS	
CLR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

X = UNSPECIFIED
↑ RISING
↓ FALLING

EL5VL029

Figure 4-22. Dual Retriggerable Monostable Multivibrator MVC-1 (74123J), Logic Symbol and Pin Arrangement.

i. Dual Monostable Multivibrator With Schmitt-Trigger Inputs MVD (74221) (fig. 4-23). The MVD module contains two one-shot multivibrators. Each multivibrator has a negative-transition-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input. The truth table on figure 4-23 provides MVD module output response for the various input combinations.

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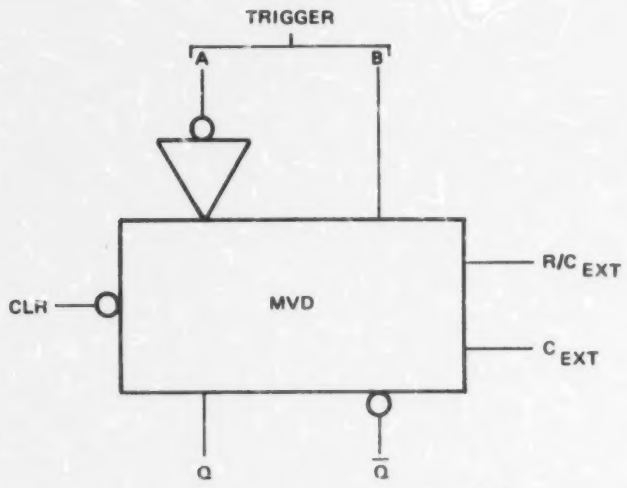

VCC – PIN 16
GND – PIN 8

PIN ARRANGEMENT

CIRCUIT NO	PIN NO						
	A	B	CLR	$\overline{Q}$	Q	C_{EXT}	R/C_{EXT}
1	1	2	3	4	13	14	15
2	9	10	11	12	5	6	7

TRUTH TABLE

INPUTS			OUTPUTS	
CLR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔

H = HIGH LEVEL
L = LOW LEVEL
X = DON'T CARE
↑ = POSITIVE TRANSITION
↓ = NEGATIVE TRANSITION

EL5VL030

Figure 4-23. Dual Monstable Multivibrator With Schmitt-Trigger Inputs MVD (74221), Logic Symbol and Pin Arrangement.

j. Dual Monostable Multivibrator With Schmitt-Trigger Inputs MVDK-1 (74LS221) (fig. 4-24). The MVDK-1 module contains two one-shot multivibrators. Each multivibrator has a negative-transition-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input. The truth table on figure 4-24 provides MVDK-1 module output response for the various input combinations.

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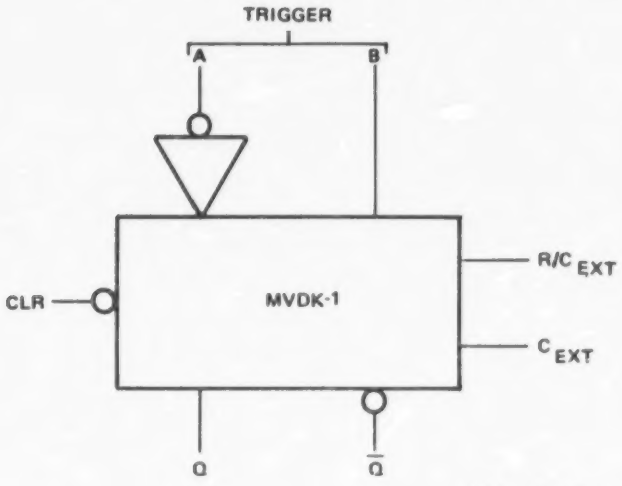

PIN ARRANGEMENT

CIRCUIT NO	PIN NO						
	A	B	CLR	$\overline{Q}$	Q	C_{EXT}	R/C_{EXT}
1	1	2	3	4	13	14	15
2	9	10	11	12	5	6	7

TRUTH TABLE

INPUTS			OUTPUTS	
CLR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⊓	⊔
H	↓	H	⊓	⊔

H = HIGH LEVEL
L = LOW LEVEL
X = DON'T CARE
↓ = POSITIVE TRANSITION
↓ = NEGATIVE TRANSITION

EL5VL031

Figure 4-24. Dual Monstable Multivibrator With Schmitt-Trigger Inputs MVDK-1 (74LS221), Logic Symbol and Pin Arrangement.

k. Dual Voltage-Controlled Oscillator OSAK-1 (74LS124) (fig. 4-25). The OSAK-1 module contains two fully independent voltage-controlled oscillators. The output frequency of each oscillator is established by an external capacitor in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. An enable input is provided, that can be used to start or stop the output pulses when it is low or high, respectively. Duty cycle of the output pulses is fixed at 50 ±5 percent. Separate supply-voltage- and ground-pins are provided for the digital logic and for the oscillator/range control circuits, so that effective isolation can be accomplished in the system. The oscillator can be set to operater at any frequency between 0.12 Hz and 85 MHz. The output frequency can be determined as follows:

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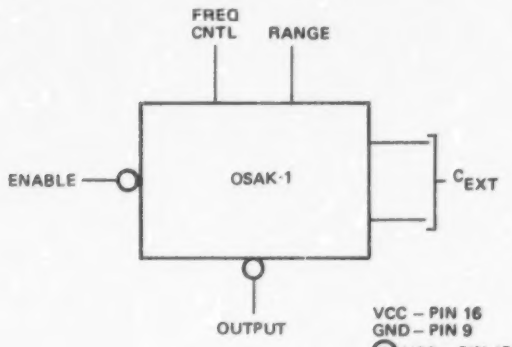
$$f_0 = \frac{500}{C_{EXT}}$$

where: f_0 = output frequency in MHz
C_{EXT} = external capacitance in pF



PIN ARRANGEMENT

CIRCUIT NO	PIN NO				
	FREQ CNTL	RANGE	C_{EXT}	ENABLE	OUTPUT
1	2	3	4, 5	6	7
2	1	14	12, 13	11	10

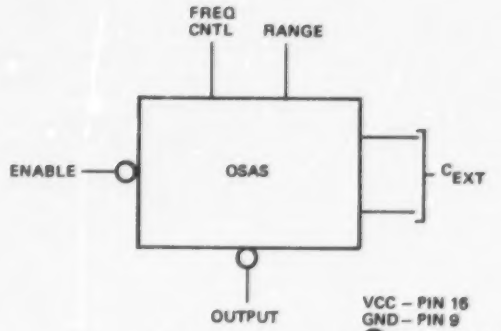
EL5VL032

Figure 4-25. Dual Voltage-Controlled Oscillator OSAK-1 (74LS124), Logic Symbol and Pin Arrangement.

l. Dual Voltage-Controlled Oscillator OSAS (74S124) (fig. 4-26). The OSAS module contains two fully independent voltage-controlled oscillators. The output frequency of each oscillator is established by an external capacitor in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. An enable input is provided that can be used to start or stop the output pulses when it is low or high, respectively. Duty cycle of the output pulses is fixed at 50 ±5 percent. Separate supply-voltage- and ground-pins are provided for the digital logic and for the oscillator/range control circuits, so that effective isolation can be accomplished in the system. The oscillator can be set to operate at any frequency between 0.12 Hz and 85 MHz. The output frequency can be determined as follows:

$$f_0 = \frac{500}{C_{EXT}}$$

where: f_0 = output frequency in MHz
C_{EXT} = external capacitance in pF



PIN ARRANGEMENT

CIRCUIT NO	PIN NO				
	FREQ CNTL	RANGE	C_{EXT}	ENABLE	OUTPUT
1	2	3	4, 5	6	7
2	1	14	12, 13	11	10

EL5VL033

Figure 4-26. Dual Voltage-Controlled Oscillator OSAS (74S124), Logic Symbol and Pin Arrangement.

m. Potentiometer Module REA103 (3099-1-103) (fig. 4-27). The potentiometer module contains a 10-kilohm potentiometer and is mounted with IC type pins. The module provides bias adjustment for voltage-controlled oscillators.

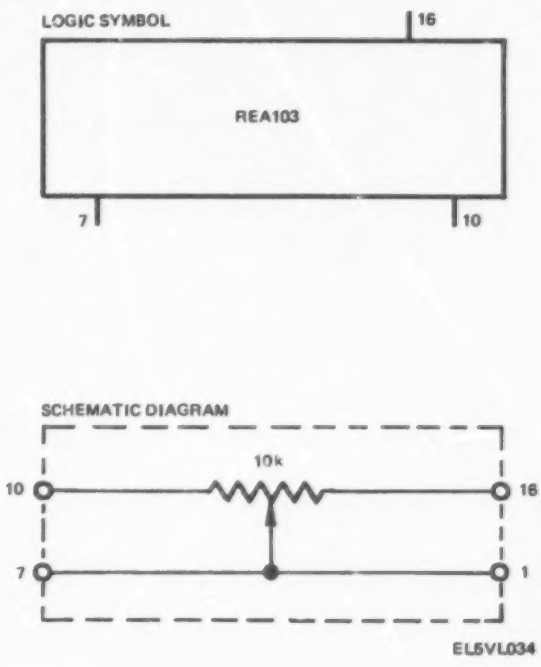


Figure 4-27. Potentiometer Module REA103 (3099-1-103), Logic Symbol and Schematic Diagram.

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25,

n. Resistor Network RES102 (899-1-R1K) (fig. 4-28). The RES102 module contains 13 1000-ohm resistors. These resistors are used to provide tieoff for circuits.

o. Resistor Network REV102 (916C102X5PD) (fig. 4-29). The REV102 module contains 14 1000-ohm resistors. These resistors are used to provide tieoff for various circuits.

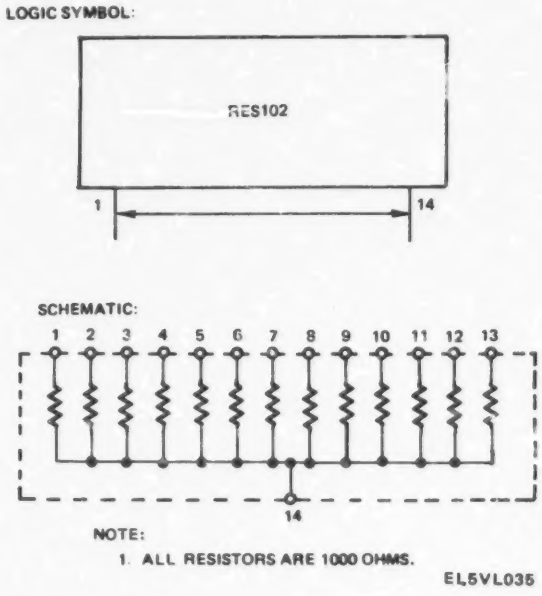

Figure 4-28. Resistor Network RES102 (899-1-R1K), Logic Symbol and Schematic Diagram.

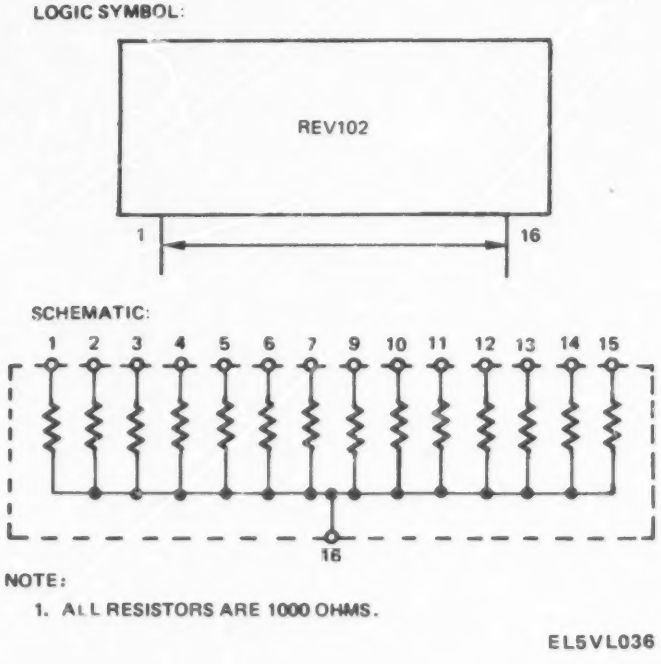

Figure 4-29. Resistor Network REV102 (916C102X5PD), Logic Symbol and Schematic Diagram.

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p. Resistor Network RES822 (899-1-R8.2K) (fig. 4-30). The RES822 module contains 13 8.2-kilohm resistors. These resistors are used to provide tieoff for various circuits.

q. Resistor Network REV151 (916C151XPE) (fig. 4-31). The REV151 module contains 14 identical resistors. These resistors are used to provide tieoff for circuits.

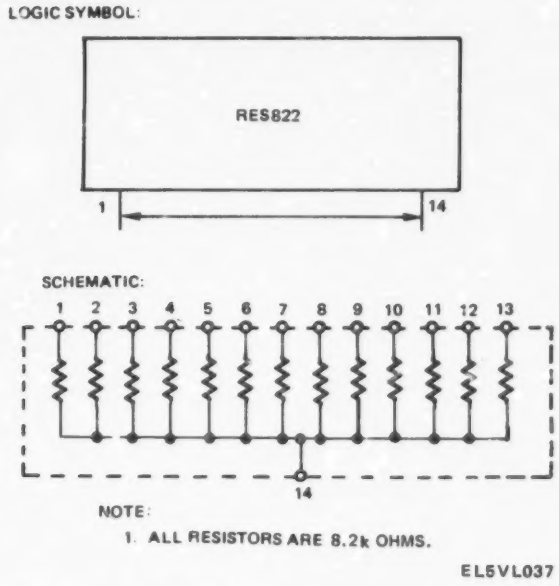

Figure 4-30. Resistor Network RES822 (899-1-R8.2K), Logic Symbol and Schematic Diagram.

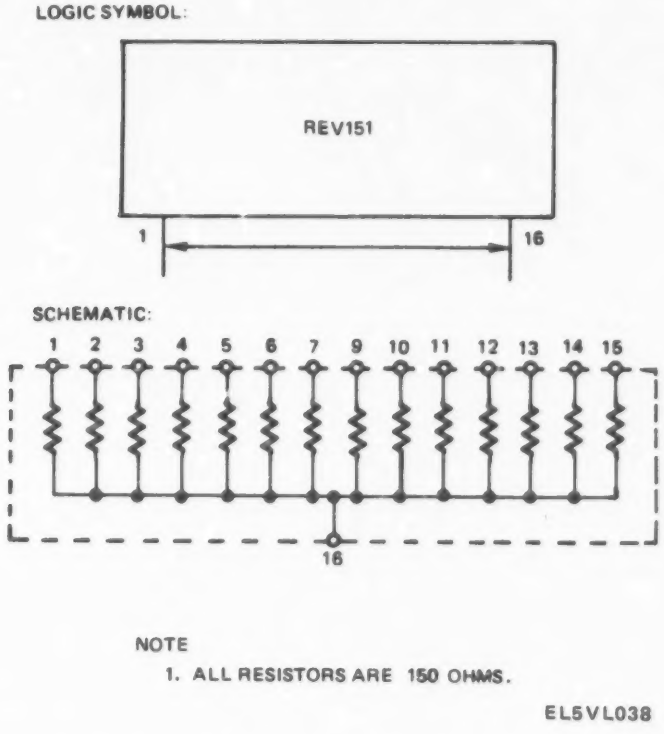

Figure 4-31. Resistor Network REV151 (916C151XPE), Logic Symbol and Schematic Diagram.

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r. Resistor Network REV223 (916C223XPE), (fig. 4-32). The REV223 module contains 14 identical resistors. These resistors are used to provide tieoff for circuits within the system status control console (SSCC).

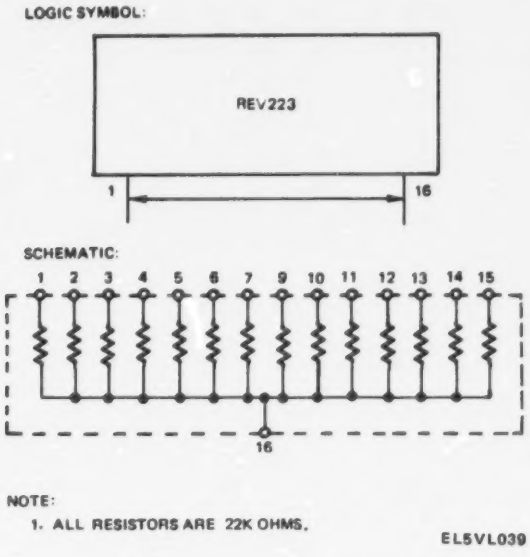

Figure 4-32. Resistor Network REV 223 (916C223XPE), Logic Symbol and Schematic Diagram.

s. Resistor/Capacitor Networks TER1 and TER2 (398-14942-4, -3) (fig. 4-33). Each TER1 and TER2 resistor/capacitor network contains resistors and capacitors that are used in conjunction with logic circuits within the system status and control console (SSCC). Values for the resistors and capacitors are shown in figure 4-33.

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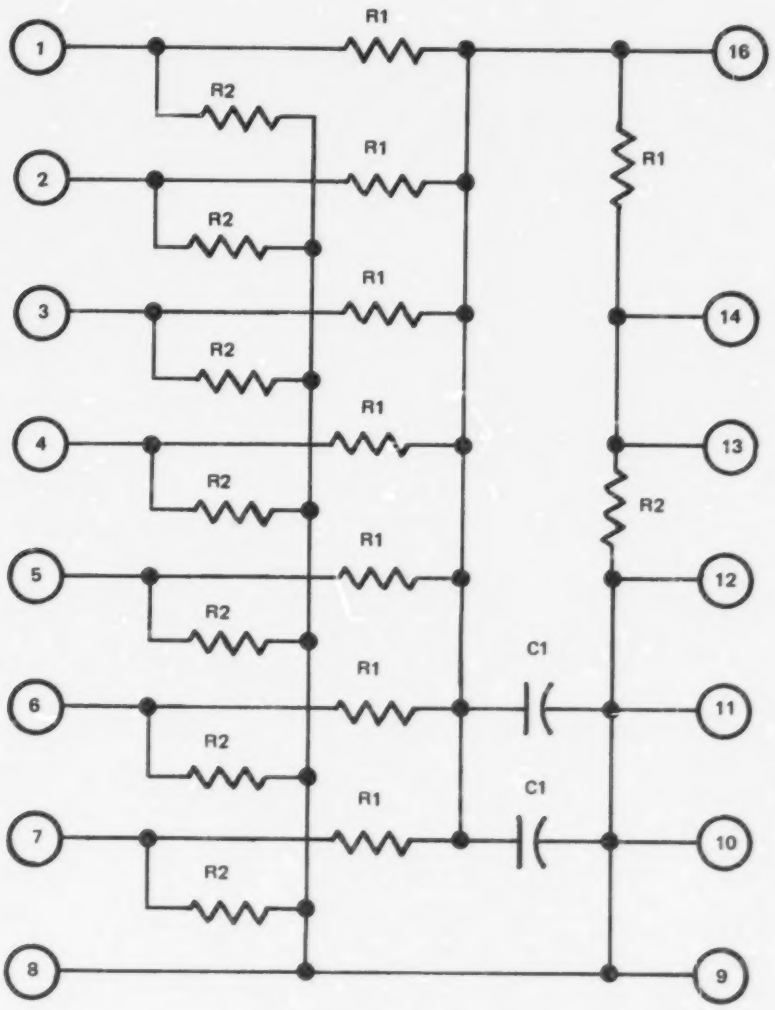

COMPONENT VALUE AND TOLERANCES

MODULE	R1	R2	C1
TER 1	1.2k 5%	1k 5%	47000pF 20%
TER 2	1.2k 5%	100Ω 5%	47000pF 20%

EL5VL040

Figure 4-33. Resistor/Capacitor Networks TER1 and TER2 (398-14942-4, -3), Schematic Diagram and Pin Arrangement.

t. Hex Inverter, 1GK-1 (74LS04) (fig. 4-34). The 1GK-1 module contains six inverters. Application of a high to the input produces a low at the output. Application of a low at the input produces a high at the output.

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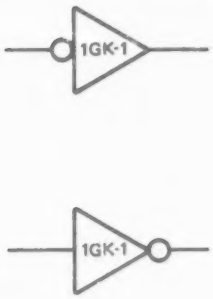


VCC – PIN 14
GND – PIN 7

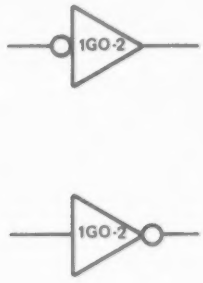
PIN ARRANGEMENT

CIRCUIT NO	PIN NO	
	INPUTS	OUTPUTS
1	1	2
2	3	4
3	5	6
4	9	8
5	11	10
6	13	12

EL5VL041

Figure 4-34. Hex Inverter 1GK-1 (74LS04), Logic Symbol and Pin Arrangement.

u. Hex Inverter 1GO-2 (7406) (fig. 4-35). The 1GO-2 module contains six inverter buffer/drivers with open-collector, high-voltage outputs. Application of a high to the input produces a low at the output. Application of a low to the input produces a high at the output.



VCC – PIN 14
GND – PIN 7

PIN ARRANGEMENT

CIRCUIT NO	PIN NO	
	INPUTS	OUTPUTS
1	1	2
2	3	4
3	5	6
4	9	8
5	11	10
6	13	12

EL5VL042

Figure 4-35. Hex Inverter 1GO-2 (7406), Logic Symbol and Pin Arrangement.

v. Hex Buffer/Driver 1QO-1 (7407) (fig. 4-36). The 1QO-1 module contains six independent circuits. Each circuit provides an open-collector buffer/driver with high-voltage output.

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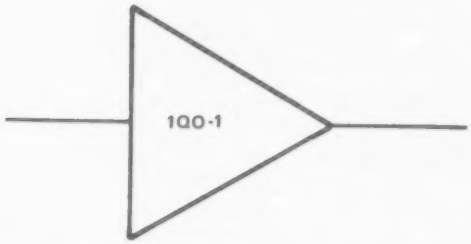


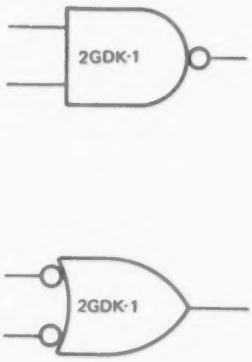
PIN ARRANGEMENT

CIRCUIT NO	PIN NO	
	INPUTS	OUTPUTS
1	1	2
2	3	4
3	5	6
4	9	8
5	11	10
6	13	12

EL5VL043

Figure 4-36. Hex Buffer/Driver 1QO-1 (7407), Logic Symbol and Pin Arrangement.

w. Quadruple 2-Input NAND Buffer 2GDK-1 (74LS37) (fig. 4-37). The 2GDK-1 module contains four 2-input logic gates. Application of highs to both inputs produces a low output. Application of a low to either input produces a high output.



VCC – PIN 14
GND – PIN 7

PIN ARRANGEMENT

CIRCUIT NO	PIN NO	
	INPUTS	OUTPUTS
1	1, 2	3
2	4, 5	6
3	9, 10	8
4	12, 13	11

EL5VL044

Figure 4-37. Quadruple 2-Input NAND Buffer 2GDK-1 (74LS37), Logic Symbol and Pin Arrangement.

x. Quadruple 2-Input Gate 2GK-1 (74LS00) (fig. 4-38). The 2GK-1 module contains four 2-input logic gates. Application of highs to both inputs of the gate produces a low output. Application of a low to one or both inputs of the gate produces a high output.

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VCC – PIN 14
GND – PIN 7

PIN ARRANGEMENT

CIRCUIT NO	PIN NO	
	INPUTS	OUTPUTS
1	1, 2	3
2	4, 5	6
3	9,10	8
4	12,13	11

EL5VL045

Figure 4-38. Quadruple 2-Input Gate 2GK-1 (74LS00), Logic Symbol and Pin Arrangement.

y. Dual 2-Wide 2-Input AND-OR-Invert Gate 2QNK-1 (74LS51) (fig. 4-39). The 2QNK-1 module contains two AND-OR-invert circuits. Application of highs to both inputs of either AND gate produces a low output at Y. Application of a low to either input of both AND gates produces a high output at Y.

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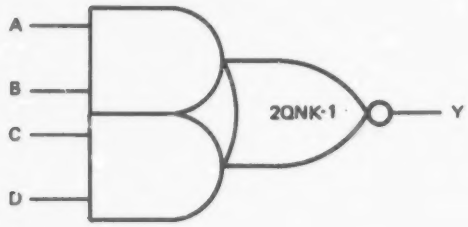


FUNCTION:

$Y = \overline{(A + B)}\ \overline{(C + D)}$

$\overline{Y} = (AB) + (CD)$

VCC – PIN 14
GND – PIN 7
NC – PINS 11, 12

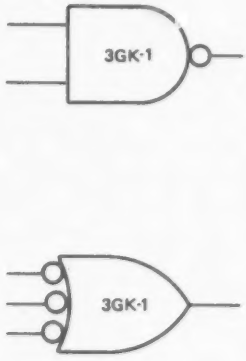
PIN ARRANGEMENT

CIRCUIT NO	PIN NO				
	INPUTS				OUTPUTS
	A	B	C	D	Y
1	2	3	4	5	6
2	9	10	1	13	8

EL5VL046

Figure 4-39. Dual 2-Wide 2-Input AND-OR-Invert Gate 2QNK-1 (74SL51), Logic Symbol and Pin Arrangement.

z. Triple 3-Input Gate 3GK-1 (74LS10) (fig. 4-40). The 3GK-1 module contains three 3-input logic gates. Application of highs to all three inputs of the gate produces a low output. Application of a low to one or more inputs of the gate produces a high output.



VCC – PIN 14
GND – PIN 7

PIN ARRANGEMENT

CIRCUIT NO	PIN NO	
	INPUTS	OUTPUTS
1	1, 2, 13	12
2	3, 4, 5	6
3	9, 10, 11	8

EL5VL047

Figure 4-40. Triple 3-Input Gate 3GK-1 (74LS10), Logic Symbol and Pin Arrangement.

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aa. Synchronous 4-Bit Counter 4BCB (74161) (fig. 4-41). The 4BCB module is a synchronous counter which can be preset for a given output level or can be free-running for incrementally counting from $(0000)_2$ to $(1111)_2$. The counter provides a carry, output signal each time a count of $(1111)_2$ is reached. This output is used in high-speed counting schemes where counters are cascaded and the carry, output signal provides the enabling signal for the next counter stage. The counter is set to $(0000)_2$ when the clear input is low regardless of the level of the other signal inputs. When the clear signal is high, the counter is enabled when the P and T, enable inputs are high. On each positive transition of the clock signal, the counter is incremented by one. A load input is provided and when the load signal is low, on the next transition of the clock, data inputs DA, DB, DC, and DD are transferred to the outputs. When the load signal returns to a high level, counting continues until a count of $(1111)_2$ is reached, at which time the counter returns to $(0000)_2$.

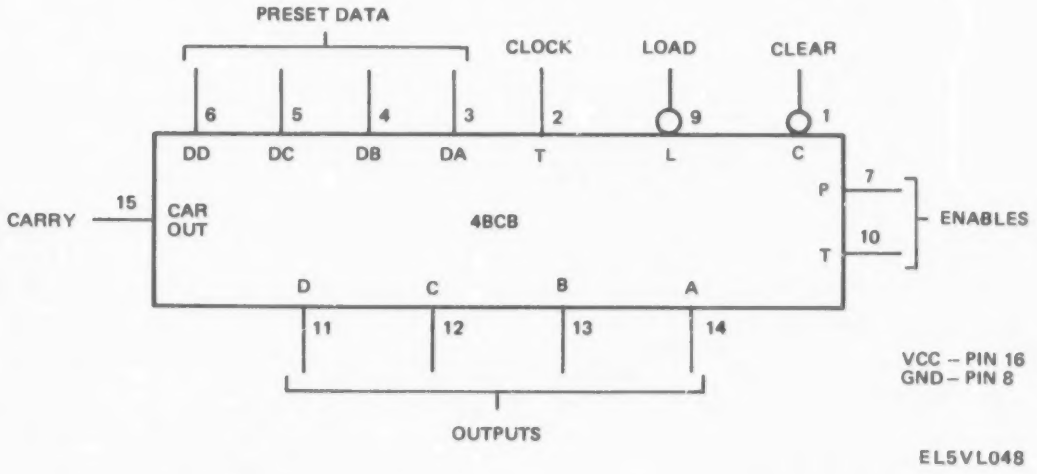

Figure 4-41. Synchronous 4-Bit Counter 4BCB (74161), Logic Symbol and Pin Arrangement.

ab. Synchronous 4-Bit Counter 4BCBK-1 (74LS161) (fig. 4-42). The 4BCBK-1 module is a synchronous counter which can be preset for a given output level or can be free-running for incrementally counting form $(0000)_2$ to $(1111)_2$. The counter provides a carry, output signal each time a count of $(1111)_2$ is reached. THis output is used in high-speed counting schemes where counters are cascaded and the carry, output signal provides the enabling signal for the next counter stage. The counter is set to $(0000)_2$ when the clear input is low regardless of the level of the other subject inputs. When the clear signal is high, the counter is enabled when the P and T, enable inputs are high. On each positive transition of the clock signal, the counter is incremented by one. A load input is provided and when the load signal is low, on the next transition of the clock, data inputs DA, DB, DC and DD are transferred to the outputs. When the load signal returns to a high level, counting continues until a count of $(1111)_2$ is reached, at which time the counter returns to $(0000)_2$.

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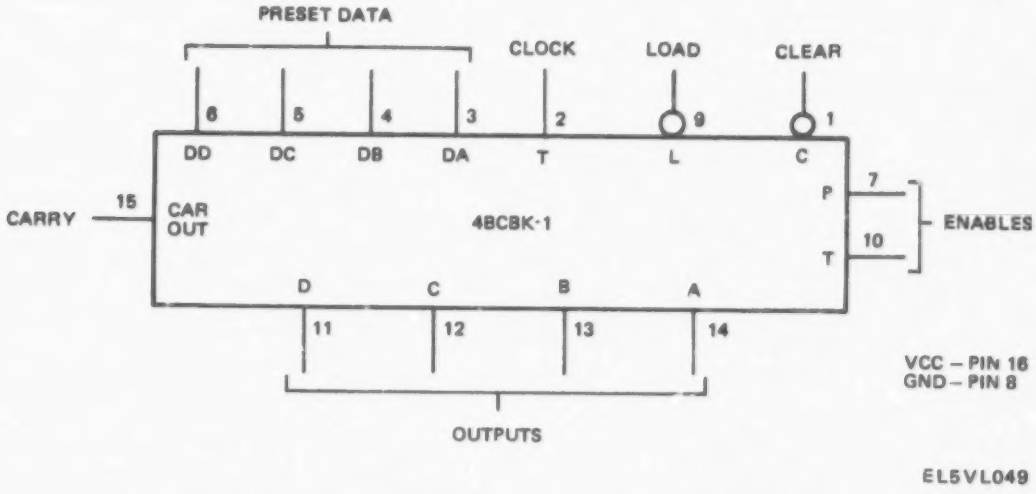
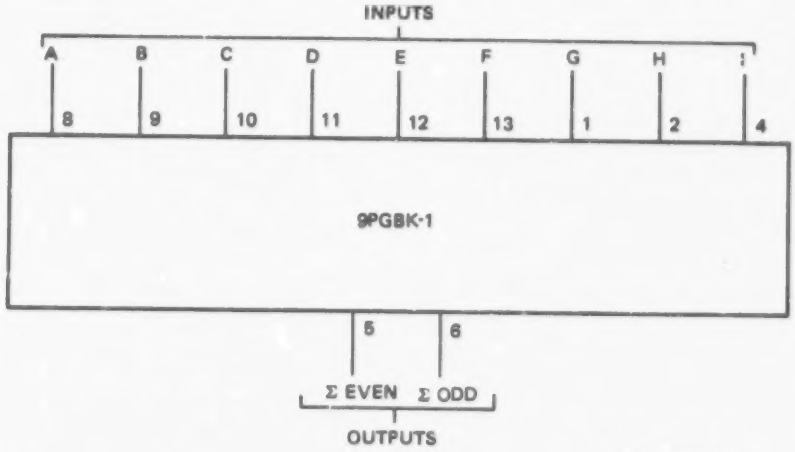


Figure 4-42. Synchronous 4-Bit Counter 4BCBK-1 (74LS161), Logic Symbol and Pin Arrangement.

ac. 9-Bit Parity Generator/Checker 9PGBK-1 (74LS280) (fig. 4-43). The 9PGBK-1 module contains one 9-bit parity generator/checker circuit. The circuit generates either odd or even parity for the nine input data lines. Application of an even number of high inputs produces a high output at pin 5 and a low output at pin 6. Application of an odd number of high inputs produces a low output at pin 5 and a high output at pin 6.



FUNCTION:

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH LEVEL
L = LOW LEVEL

EL5VL050

Figure 4-43. 9-Bit Parity Generator/Checker 9PGBK-1 (74LS280), Logic Symbol and Pin Arrangement.

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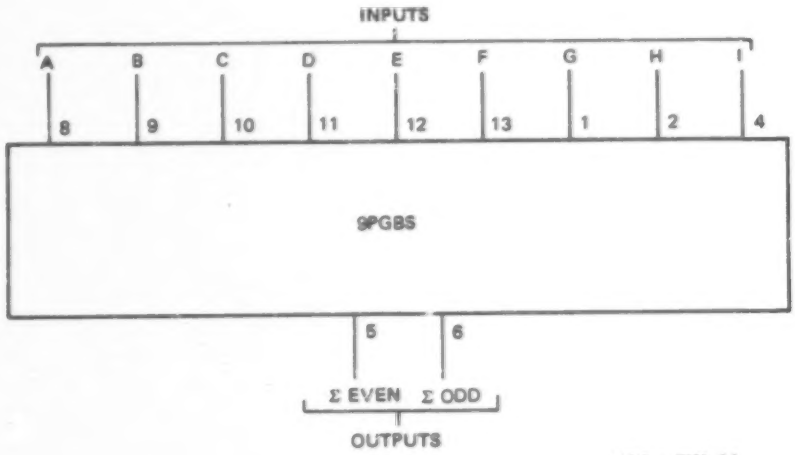
ad. 9-Bit Parity Generator/Checker 9PGBS (74S280) (fig. 4-44). The 9PGBS module contains one 9-bit parity generator/checker circuit. The circuit generates either odd or even parity for the nine input data lines. Application of an even number of high inputs produces a high output at pin 5 and a low output at pin 6. Application of an odd number of high inputs produces a low output at pin 5 and a high output at pin 6.



FUNCTION:

NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH LEVEL
L = LOW LEVEL

EL5VL051

Figure 4-44. 9-Bit Parity Generator/Checker 9PGBS (72S280), Logic Symbol and Pin Arrangement.

ae. Quadruple 2-Input Gate 2IK-1 (74LS32) (fig. 4-45). The 2IK-1 module contains four 2-input logic gates. Application of a high to either input of the gate produces a high output. Application of a low to both inputs produces a low input.

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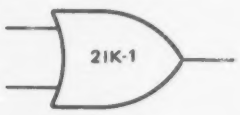

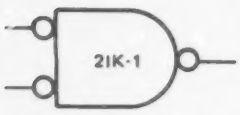

VCC – PIN 14
GND – PIN 7

PIN ARRANGEMENT

CIRCUIT NO	PIN NO	
	INPUTS	OUTPUTS
1	1, 2	3
2	4, 5	6
3	9, 10	8
4	12, 13	11

EL5VL052

Figure 4-45. Quadruple 2-Input Gate 2IK-1 (74LS32), Logic Symbol and Pin Arrangement.

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CHAPTER 5

MAINTENANCE INSTRUCTIONS

5-1. General

a. This chapter contains instructions for performing preventive and corrective maintenance operations and the associated testing procedures.

b. Maintenance includes:

(1) Preventive maintenance checks and services (para 5-3*f*).

(2) Fault isolation to a defective subassembly or major component (para 5-6).

(3) Removal and replacement procedures for defective subassemblies and components (para 5-7).

5-2. Tools, Test Equipment, and Materials Required

a. The tools and test equipment required for maintenance are listed and identified in the maintenance allocation chart, appendix C.

b. The materials required for maintenance are listed below:

(1) Oil, lubricating, general purpose (PL) (NSN 9150-00-273-2389)

(2) Lint-free cloth (NSN 7920-00-205-3453)

(3) Brush, paint, 1/2 inch width (NSN 8020-00-597-4761)

(4) Trichlorotrifluoroethane (cleaning compound).

Freon, PCA (NSN 6850-00-984-5856) or
Freon, TF (NSN 6850-00-105-3084)

(5) Detergent (NSN 7930-00-068-1669)

(6) Silicone compound (DOW Corning 340 heat sink compound) (NSN 6850-00-927-9461)

(7) Varnish, Electrical (GE Glyptal ZV-903) (NSN 5970-00-162-7523)

5-3. Preventive Maintenance

a. General. Preventive maintenance is the systematic care, inspection, and servicing of equipment to maintain it in serviceable condition, prevent breakdowns, and insure maximum operational capability. Preventive maintenance of the SSCC is the responsibility of the maintenance personnel. Preventive maintenance includes the inspection, testing, and replacement of subassemblies and components that inspection and tests indicate would probably fail before the next scheduled periodic service.

b. Preventive Maintenance Checks and Services Periods. The preventive maintenance checks and services for the SSCC are given in the following subparagraphs. These checks and services must be performed during the specified periods. Records and reports of the preventive maintenance checks and services must be made in accordance with the requirements set forth in DA Pam 738-750 (Army) or TO-00-35D-54 (Air Force) or OPNAVINST 4790.2 Vol 3 (Navy).

c. Cleaning.

(1) Clean dust and dirt from within equipment cabinet using a vacuum cleaner and dust brush.

(2) Clean cabinet exterior using a vacuum cleaner and dust brush or a clean, dry lint-free cloth.

(3) Clean smudges or stubbornly dirty surface areas by wiping with a clean, lint-free cloth moistened with detergent. Wipe dry with a clean, dry cloth.

d. Touchup Painting. Remove rust and corrosion from metal surfaces by lightly sanding with fine sandpaper. Brush two thin coats of paint on bare metal to protect it from further corrosion. Refer to the applicable cleaning and refinishing practices specified in TB 43-0118.

e. Lubrication.

(1) *Cooling fans.* The cooling fans, located in the base of each bay do not require lubrication.

(2) *Doors.*

(a) Lubricate door hinge pins on each bay door, using special preservative lubricating oil (PL), taking care not to overlubricate.

(b) Apply one or two drops to each hinge pin, and wipe away any excess lubricant, using a clean, lint-free cloth.

NOTE

To perform the following procedures, the SSCC need not be connected to a processor unit.

f. Preventive Maintenance Checks and Services. The periodic preventive maintenance checks and services and to be performed on the SSCC are listed in table 5-1.

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Table 5-1. Preventive Maintenance Checks and Services.

Item no.	Interval W[1]	Interval M[2]	Interval A[3]	Item to be inspected	Procedure	Equipment will be reported not ready (red) if:
1		o		Modification work orders (MWO's)	Check to see if any MWO's are required. Check that current MWO's have been applied and MWO numbers are stamped as required. Perform modifications or request modifications, as applicable. Refer to applicable MWO (DA Pam 310-1).	Not applicable.
2		o		Bay exterior	Clean bay exterior surfaces with vacuum cleaner and dust brush. Use mild detergent solution (NSN 7930-00-068-1669) and water, with a soft cloth, to remove any stubborn dirt accumulations para 5-3*c*). Inspect bay exterior for corrosion or need of refinishing (para 5-3*d*). Lubricate door as required (para 5-3*e*).	Not applicable.
3		o		Bay interior	Open rear door of each bay and inspect for cleanliness. Dust or vacuum as required. Inspect for damaged or loose wiring, loose connections, and evidence of component damage.	Not applicable
4	o			Blowers in bays A1, A3, and A5	Open rear bay doors and check airflow up through blowers located in each bay. If noise or vibration is excessive, replace blowers (para 5-7*l*).	Blower assembly needs to be replaced.
5	o			Air filter	Using a vacuum cleaner, remove dust and dirt from inlet (lower) side of filter.	Not applicable.
6	o			Printed circuit cards	Check logic pans of each bay to determine that all circuit cards are fully seated in their receptacles. NOTE Do not check PRINTER 1 and 2 or CARD switches of processor panel 2, as these are not used.	
7	o			Rocker and pushbutton switches	Make sure that all rocker switches and pushbutton switches operate freely.	
8		o		Air filter	*a.* Prepare a mild detergent solution; soak filter in solution (submerged) for a few minutes. Thoroughly wash filter by agitating, and raising and lowering filter in solutions. *b.* Rinse filter in running water, inverting filter several times to allow water to flow through filter in both directions. No trace of dirt or detergent should be noticeable. *c.* Shake out loose moisture from filter. *d.* Allow filter to air-dry. If required, drying may be accelerated by using a low pressure source (5 lb/in^2) of dry compressed air. *e.* Return filter to original position in filter slide assembly and close rear door of equipment cabinet.	Not applicable

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Table 5-1. Preventive Maintenance Checks and Services—Continued.

Item no.	Interval W[1]	Interval M[2]	Interval A[3]	Item to be inspected	Procedure	Equipment will be reported not ready (red) if:
9		o		Electrical check	Perform dc power supply checks as outlined in paragraph 5-5*b*.	Power supply does not pass operational test.
10	o			Lamp test	Depress LAMP TEST switch on each processor panel and observe that all required indicator lamps and push-button switch faceplates are illuminated (para 3-2*e*). If necessary, replace any defective lamps. (fig. FO-3, para 5-7*b* and 5-7*e*(1)).	Not applicable
11		o		Publications	Check to see that all publications are complete and current (DA Pam 310-1).	Not applicable

1. W = Weekly, 2. M = Monthly, 3. Y = Yearly

5-4. Corrective Maintenance

Corrective maintenance consists of procedures for the identification and correction of conditions that have caused a specific malfunction. These procedures comprise troubleshooting procedures; calibration, adjustment, and alinement procedures; and removal and replacement procedures (described in detail only where these are not obvious). In addition to these procedures, this section includes a description of the maintenance aids available, and parts location diagrams for components of the unit. Maintenance information for the printed circuit cards is provided in TM 11-5895-402-15/1, TM 11-5895-402-15/2, TM 11-5895-554-15/1, TM 11-5895-554-15/2, and TM 11-5895-554-15/3.

5-5. Operational Test

a. General. The tests contained in this paragraph are designed to aid in the localization and isolation of a defective circuit or component in the SSCC. Perform the tests listed in the procedures and, when an abnormal indication is noted, refer to the applicable troubleshooting procedure given in paragraph 5-6.

CAUTION

Operational tests are not provided nor should they be performed for the SSCC SAM start and manual connect functions. Testing of these functions would affect on-line system operations. Should a failure be suspected in these functions, refer to the troubleshooting techniques contained in paragraph 5-6*b*.

b. Operational Test Procedure (table 5-2).

Table 5-2. Operational Test Procedure

Step no.	Test	Test procedure	Normal indication
1	SSCC dc power checks	**SSCC POWER SUPPLIES** *a.* Turn on voltmeter ME-303A/U (Hewlett-Packard Model 410C, or equivalen) and Oscilloscope AN/USM-281C (or equivalent) with Probe P-6006 (or equivalent). Allow at least 15minutes for warmup and stabilization before proceeding. *b.* Zero the vtvm and set controlto the 30-volt range. *c.* On the front panel of the +16V dc power supply (fig. 3-5), connect the DC test lead of the vtvm to terminal TB1-5 and the common test lead to terminal TB1-10. *d.* Observe the vtvm indication, being careful to look straight downward at the needle and scale to avoid parallax errors in the observation.	The indication should be 16 ±0.3 V dc. If not in tolerance, adjust the VOLTAGE ADJUST control (located on the power supply front panel) to bring the vtvm indication within tolerance.

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Table 5-2. Operational Test Procedure—Continued

Step no.	Test	Test procedure	Normal indication
1 (Cont.)		*e.* Connect the channel 1 vertical input of the oscilloscope to terminal TB1-5 (positive) and the ground lead to terminal TB1-10 (negative).	The ripple voltage should not exceed 80 mV peak-to-peak.
		f. On the front panel of the −10 V dc power supply (fig. 3-5), connect the DC test lead of the vtvm to terminal TB1-10 and the common test lead to terminal TB1-5.	
		g. Observe the vtvm indication, being careful to look straight down at the needle and scale to avoid parallax errors in the observation.	The indication should be 10 V dc ±0.2 V dc. If not in tolerance, adjust the VOLTAGE ADJUST control (located on the power supply front panel) to bring the vtvm indication within tolerance.
		h. Connect channel 1 vertical input of the oscilloscope to terminal TB1-10 (negative) and the ground lead to terminal TB1-5 (positive).	The ripple voltage should not exceed 50 mV peak-to-peak.
		i. On the front panel of the −27 V dc power supply (fig. 3-5), connect the DC test lead of the vtvm to terminal E3 and the common test lead to terminal E2.	
		j. Observe the vtvm indication.	The indication should be 27 V dc ±1.4 V dc. If not in tolerance, adjust the VOLTAGE ADJUST control (located on the power supply front panel) to bring the vtvm indication within tolerance.
		k. Connect channel 1 vertical input of the oscilloscope to terminal E3 (negative) and ground lead to terminal E2 (positive).	The ripple voltage should not exceed 810 mV peak-to-peak.
		l. To adjust the −5 V dc power supply PS1, connect the vtvm common test lead to E2 on the SSCC logic board (fig. 1-5) and the DC test lead to E6.	The output voltage should be 5.0 ±0.5 V dc. If out of tolerance, adjust −5 V dc adjustment (fig. 5-2) for correct indication.
		m. Connect oscilloscope to E6 and measure −5 V dc peak-to-peak ripple voltage.	The ripple voltage should not exceed 1 mV peak-to-peak.
		n. To adjust the +5 V dc power supply PS2, connect the vtvm common test lead to E2 on the SSCC logic board (fig. 1-5) and the DC test lead to E1.	The output voltage should be 5.0 ±0.5 V dc. If out of tolerance, adjust +5 V dc adjustment (fig. 5-2) for correct indication.
		o. Connect oscilloscope to E1 and measure +5 V dc power supply peak-to-peak ripple voltage.	The ripple voltage should not exceed 1 mV peak-to-peak.
		PROCESSOR PANEL	
2	−5.6 V dc	Measure between E2 (−) and E1 (ground) on power supply (FO-5).	−5.6 ±0.5 V dc.
3	+5.1 V dc power	Measure between E4 (+) and E1 (ground) on power supply.	+5.1 ±0.5 V dc.
4	RO indicator drive circuit (test applies to all processor status indicator driver circuits)	*a.* Connect a jumper between ground (B01-08) and B01-11.	*a.* RO lamp lights.
		b. Remove jumper connection.	*b.* RO lamp extinguishes.
		NOTE	
	For the following tests the control panel should be opened so that both sides are accessible.		
5	T (I) switch operation (test applies to all T rocker switches)	*a.* Set switch T (I) to 1 position.	*a.* +5.1 ±0.5 V dc between S32-2 and ground.
		b. Set switch T (I) to 0 position.	*b.* 0.0 V dc between S32-2 and ground.
6	KA (V15) switch operation (test applies to all KA rocker switches).	*a.* Set switch KA (V15) to 1 position.	*a.* −5.6 ±0.5 V dc between S49-2 and ground. +5.1 ±0.5 V dc between S49-5 and ground.
		b. Set swich KA (V15) to 0 position.	*b.* −5.1 ±0.5 V dc between S49-2 and ground. −5.6 ±0.5 V dc between S49-5 and ground.

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Table 5-2. Operational Test Procedure—Continued

Step no.	Test	Test procedure	Normal indication
7	FAULT ACTION switch operation (test also applies to OPERATE rocker switch).	a. Set FAULT ACTION switch to INTER position.	a. −10 ±0.1 V dc between S67-3 and ground, and S67-6 and ground.
		b. Set FAULT ACTION switch to OVRD position.	b. −10 ±0.1 V dc between S67-3 and ground. +5.1 ±0.5 V dc between S67-6 and ground.
		c. Set FAULT ACTION switch to STOP position.	c. +5.1 ±0.5 V dc between S67-3 and ground. −1.0 ±0.5 V dc between S67-6 and ground.
8	CLEAR (TAPE 1) transmit circuit (test applies to all TAPE CLEAR, HALT, and CONT transmit circuits).	a. Depress and hold CLEAR (TAPE 1) switch.	a. −1.0 ±0.5 V dc between C38-10 and C38-8 (ground).
		b. Release CLEAR (TAPE 1) switch.	b. +0.5 ±0.05 V dc between C38-10 and C38-8 (ground).
9	TAPE 1 FAULT, HALT, and RUN indicator driver circuits (test applies to all TAPE indicator driver circuits).	a. Connect a jumper between C31-08 and C31-10.	a. TAPE 1 FAULT and TAPE 1 RUN indicators remain lit. TAPE 1 HALT indicator extinguishes.
		b. Remove jumper connected in *a* and connect it between C31-08 and C31-12.	b. TAPE 1 FAULT indicator extinguishes. TAPE 1 HALT and TAPE 1 RUN indicators are lit.
		c. Remove jumper connected in *b* and connect between C31-08 and C31-14.	c. TAPE 1 HALT and TAPE 1 FAULT indicators are lit. TAPE 1 RUN indicator is extinguished.
		NOTE Remove jumper after completion of this test.	
10	SCANNER LOCK switch and indicator operation (test also applies to TGL AS ACW, TGL AS INST, RETAIN INST, and MEMORY PROT OVRD switch/indicators).	a. Depress SCANNER LOCK switch/indicator.	a. SCANNER LOCK indicator illuminates. +5.1 ±0.5 V dc between S64-3 and ground.
		b. Depress SCANNER LOCK switch/indicator.	b. SCANNER LOCK indicator extinguishes. −10 ±1.0 V dc between S64-3 and ground.
11	PROC STOP switch and indicator operation (test also applies to IOS STOP, and STOP ON STORE ONLY switch/indicators).	a. Depress PROC STOP switch/indicator.	a. PROC STOP indicator illuminates +5.1 ±0.5 V dc between S33-2 and ground.
		b. Depress PROC STOP switch/indicator.	b. PROC STOP indicator extinguishes. 0.0 V dc between S33-2 and ground.
12	RUN switch and indicator operation.	a. Depress RUN switch/indicator.	a. RUN indicator illuminates. +5.1 ±0.5 V dc between S55-3 and ground. −10 ±1.0 V dc between S55-1 and ground.
		b. Depress RUN switch/indicator.	b. RUN indicator extinguishes. +5.1 ±0.5 V dc between S55-1 and ground. −10 ±1.0 V dc between S55-3 and ground.
		NOTE When testing SET SCANNER, CLEAR, LOAD PA, DISPLAY, AUTO LOAD, and STORE momentary-action switches, the RUN switch must be off.	
13	CLEAR momentary-action switch operation (test also applies to SET SCANNER, LOAD PA, ADVANCE, DISPLAY, AUTO LOAD, and STORE momentary-action switches).	a. Depress and hold CLEAR switch.	a. +5.1 ±0.5 V dc between S57-3 and ground.
		b. Release CLEAR switch.	b. −10 ±0.1 V dc between S57-3 and ground.

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Table 5-2. Operational Test Procedure—Continued

Step no.	Test	Test procedure	Normal indication
14	INTERRUPT momentary-action switch operation.	a. Depress and hold INTERRUPT switch.	*a.* +5.1 ±0.5 V dc between S61-3 and ground −10 ±0.1 V dc between S61-1 and ground.
		b. Release INTERRUPT switch.	*b.* +5.1 ±0.5 V dc between S61-1 and ground. −10 ±0.1 V dc between S61-3 and ground.
15	LAMP TEST circuitry.	Depress LAMP TEST switch.	All required indicators on control panel light (para 3-2*g*).

5-6. Troubleshooting Procedures (table 5-3)

a. SSCC Processor Maintenance Circuits. To fault isolate the processor panels, configure the SSCC as directed for the operational tests of paragraph 5-5, and note the apparent trouble symptom. Locate the symptom in the troubleshooting chart, note the probable trouble, and take the indicated corrective measure. Whenever a subassembly or component is replaced, repeat the applicable operational test procedure to verify proper operation of the replacement item. Before performing the corrective measures listed for a particular symptom, inspect all wiring and connections (including connector boards) which affect the problem area. When the symptom given involves a faulty indicator circuit, check the indicator lamp before proceeding with the corrective measures given. Normally, a fault occurring on the subsystem status panel is immediately isolated to the logic circuits associated with the status display for the affected system. Specific situations are described below.

NOTE

The troubleshooting procedures below are given once for each type of circuit. These procedures are applicable to all other circuits of the same type.

Table 5-3. Processor Panel, Troubleshooting Chart.

Item no.	Malfunction	Probable cause	Corrective action
1	No −5.6 V dc power at E2 on processor panel.	Defective power supply component.	Measure for −10 ±0.1 V dc at E3. If incorrect, fault is at power source. If present, check R1 and CR1 and replace defective component.
2	No +5.1 V dc power at E4.	Defective power supply component.	Measure for −16 ±1.0 V dc at E5. If incorrect, fault is at power source. If present, check R2 and CR2 and replace defective component.
3	RO indicator does not light.	*a.* Defective lamp driver.	*a.* Connect a jumper between B01-08 and B01-11. Measure the voltage at B01-10. If −5.0 ±0.5 V dc is measured, replace the plug-in card at B02.
		b. Defective inverter.	*b.* If −5 ±0.5 V dc was not measured above, replace the plug-in card at B01.
4	Faulty operation of T(I) rocker switch.	Defective T(I) rocker switch.	Check rocker switch S32, replace if defective.
5	Faulty operation of KA (V15) rocker switch.	Defective KA (V15) rocker switch.	Check rocker switch S49, replace if defective.
6	Faulty operation of FAULT ACTION rocker switch.	Defective FAULT ACTION rocker switch.	Check rocker switch S67, replace if defective.
7	Abnormal output level from CLEAR (TAPE 1) transmit circuit.	*a.* Defective CLEAR (TAPE 1) momentary-action switch.	*a.* At S73-2, measure for +5.1 ±0.5 V dc with CLEAR (TAPE 1) switch activated and for −5.6 ±0.5 V dc with switch inactivated. If either of these conditions are not met, replace momentary-action switch S73.

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Table 5-3. Processor Panel, Troubleshooting Chart—Continued.

Item no.	Malfunction	Probable cause	Corrective action
7 (Cont.)		*b.* Defective bias clamping board.	*b.* At C38-11, measure for between 0 and 0.5 V dc with CLEAR (TAPE 1) switch activated and for −5.6 ±0.5 V dc with switch inactivated. If these conditions are not met, replace the plug-in card at C61.
		c. Defective lie transmitter.	*c.* If both of the above conditions were met, replace the plug-in card at C38.
8*a*	Faulty operation of TAPE 1 FAULT (or TAPE 1 HALT indicator.	Defective lamp driver or line receiver.	Connect a jumper between C31-13 (C31-11) and C31-08. Measure for −5 ±0.5 V dc at C31-12 (C31-10). If −5 ±0.5 V dc is measured, replace the plug-in card at C33. If −5 ±0.5 V dc is not measured, replace the plug-in card at C31.
8*b*	Faulty operation of TAPE 1 indicator.	*a.* Defective lamp driver.	*a.* Connect jumpers from C31-08 (ground) to C31-10, C31-12, and C31-14. Measure for −5 ±0.5 V dc at C33-14. If −5 ±0.5 V dc is measured, replace the plug-in card at C33. If −5 ±0.5 V dc is not measured, proceed to *b* below.
		b. Defective inverter or line receiver.	*b.* Replace the plug-in card at C32 with a known good one. Measure for −5±0.5 V dc at C33-14. If approximately −5 V dc is measured, the plug-in card at C32 was defective. If −5 ±0.5 V dc is not measured, replace the plug-in card at C31.
9*a*	Faulty operation of SCANNER LOCK indicator and alternate-action switch.	Defective SCANNER LOCK alternate-action switch.	Check alternate-action switch/indicator S64/XDS128, replace if defective.
9*b*	SCANNER LOCK indicator fails to light. Switch action normal.	Defective dropping resistor.	Check dropping resistor (R11), connecting S64-05 and XDS128-D1, replace if defective.
10*a*	Faulty operation of RUN indicator and alternate-action switch.	Defective RUN alternate-action switch.	Check alternate-action switch/indicator S55/SCS123, replace if defective.
10*b*	RUN indicator fails to illuminate. Switch action normal.	Defective dropping resistor.	Check dropping resistor (R6), connecting S55-05 and XDS123-D1, replace if defective.
11	Faulty operation of CLEAR momentary-action switch.	Defective CLEAR momentary-action switch.	Check momentary-action switch S57, replace if defective.
12	Faulty operation of INTERRUPT momentary-action switch.	Defective INTERRUPT momentary-action switch.	Check momentary-action switch S61, replace if defective.
13*a*	LAMP TEST momentary-action switch has no effect on all indicators or on complete blocks of indicators.	Defective LAMP TEST momentary-action switch.	Check momentary-action switch S59, replace if defective.
13*b*	LAMP TEST momentary-action switch has no effect on certain indicators.	Defective diode lamp test connector (CON 13).	Replace associated diode on plug-in card corresponding to affected indicator as indicated below. *Card Location* — *Indicators* PA41 — PROC through PARITY PA42 — R00 through R27 PA43 — R28 through R31; D00 through D23 PA44 — ALL INSTRUCTION REGISTER; OPERAND ADDRESS V3 through K0 PA60 — OPERAND ADDRESS V4 through V15 All PA

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b. SSCC Logic Troubleshooting Techniques. The SSCC logic associated with the fault and unit-unavailable indicators and the monitor selection is very simple and straightforward. If a failure is suspected, refer to the logic diagram (drawing 520484), figure FO-9 (module location) and the fault indicator panel logic description in chapter 4 and fault isolate, using an oscilloscope. If a failure is suspected in the SSCC logic associated with the SAM start or manual connect functions, perform the following procedures and coordinate this effort with the operations personnel.

CAUTION

Troubleshooting the SSCC logic could affect online system operations. Exercise care in performing the following procedures and coordinate this activity with operations personnel.

(1) *SAM start logic troubleshooting.*

(a) Connect an offline processor panel to an offline 102 processor.

(b) On the processor panel, set KA rocker switches to octal 102000 and set PROC STOP switch to on.

(c) On the configuration control panel, set the MON SEL switch to indicate the current online monitor.

(d) Set the MP SEL switch to indicate the offline processor used in step *(a)* above.

(e) On the SAM panel, set CSC select to indicate the current online CSC.

(f) On the current online monitor, install jumpers between ground and A14-4 and between ground and B39-13.

(g) Refer to the logic diagram (drawing 520484) and the SAM start theory of operation in chapter 4. Fault isolate using an oscilloscope, while touching the SAM panel ENABLE switch and, then, the START switch. Touching the ENABLE switch should cause the yellow ENABLE indicator to flash. Touching the START switch should cause the green START indicator to light and the yellow ENABLE indicator to go off. The ENABLE and START switches may be touched repeatedly, if necessary, while monitoring different points with the oscilloscope.

CAUTION

After completion of troubleshooting and repair, insure that the proper monitor, CSC, and MP are still connected for system operation and jumper wires are removed from the monitor.

(2) *Manual connect logic troubleshooting.*

(a) On the current online monitor, install a jumper between ground and B39-13.

(b) On the SAM panel, set CSC select to indicate 1 or 2, as desired.

(c) Refer to the logic diagram (drawing 520484) and to manual connect theory of operation in chapter 4. Fault isolate using an oscilloscope, while touching the CON CSC switch. The CON CSC switch may be touched repeatedly, if necessary, while monitoring different points with the oscilloscope.

CAUTION

After completion of troubleshooting and repair, insure that the proper CSC is still connected to system operation and that the jumper wire is removed from the monitor.

c. +5 V Dc and −5 V DC Power Supply Troubleshooting and Test.

(1) *General.* Whenever a power supply fault occurs, systematically check fuse, primary power lines, external circuit elements, and external wiring for malfunction before troubleshooting the power supply. Failures and malfunctions often can be traced to simple causes such as jumpers, supply-load connections, or fuse failure due to metal fatigue.

(2) *Troubleshooting and repair techniques.*

(a) Check transistors with an instrument that has a highly limited current capability. Observe proper polarity to avoid error in measurement. The forward transistor resistance is low but never zero; backward resistance is always higher than the forward resistance. For good transistors, the forward resistance for any junction is always greater than zero.

(b) Do not assume trouble is eliminated when only one part is replaced. This is especially true when one transistor fails, causing other transistors to fail. Replacing only one transistor and turning power on, before checking for additional defective components, could damage the replaced component.

(c) Wherever possible, use a heat sink when soldering semiconductor devices. If a heat sink tool is not available, hold the lead being soldered with a pair of pliers placed between the component and the solder joint to provide an effective heat sink.

(d) The leakage resistance obtained from a simple resistance check of a capacitor is not always an indication of a faulty capacitor. In all cases, the capacitors are shunted with resistances, some of which have low values. Only a dead short is a true indication of a shorted capacitor.

(e) If printed circuit board foil is intact but not covered with solder, it is a good contact. Do not attempt to cover with solder.

(f) Voltage measurements can be made from either side of the printed circuit board. Use a needle-point probe to penetrate to the wiring whenever a protective coating is used on the wiring. A brass

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probe can be soldered to an alligator clip adapted to the measuring instrument.

(g) Broken or damaged printed wiring is usually the result of an imperfection, strain, or careless soldering. To repair small breaks, tin a short piece of hook-up wire to bridge the break, and, holding the wire in place, flow solder along the length of wire so that it becomes part of the circuitry.

(h) When unsoldering components from the board, never pry or force loose the part; unsolder the component by using the wicking process described below, or any other acceptable method:

1. Select a 3/16 inch tinned copper braid for use as a wick; if braid is not available, select AWG No. 14 or No. 16 stranded wire with 1/2 inch insulation removed.

2. Dip the wick in liquid rosin flux.

3. Place the wick to the soldered connection and apply soldering iron to the wick.

4. When a sufficient amount of solder flows onto the wick, freeing the component, simultaneously remove iron and wick.

(i) When replacing a power series regulator transistor, an insulating wafer must be placed between the transistor and the chassis. In order to provide good thermal transfer so the transistor will not overheat, coat both sides of the insulating wafer with silicone compound (NSN 6850-00-927-9461) (Dow Corning 340 heat sink compound). Figures FO-7 and FO-8 show which transistors require application of the silicone compound.

(3) *Troubleshooting and test.* To troubleshoot and test a +5 V DC or −5 V DC power supply, remove the power supply from the SSCC (para 5-7*i*). Remove the power supply cover and connect the power supply as shown in figure 5-1. The following test equipment is required to troubleshoot and test the power supplies:

(a) Oscilloscope AN/USM-281C or equivalent.

(b) Ammeter, Direct Current ME-511/U (Weston 931-2902001) or equivalent.

(c) Differential Voltmeter TS-2843/U or equivalent.

(d) Multimeter AN/USM-223 or equivalent.

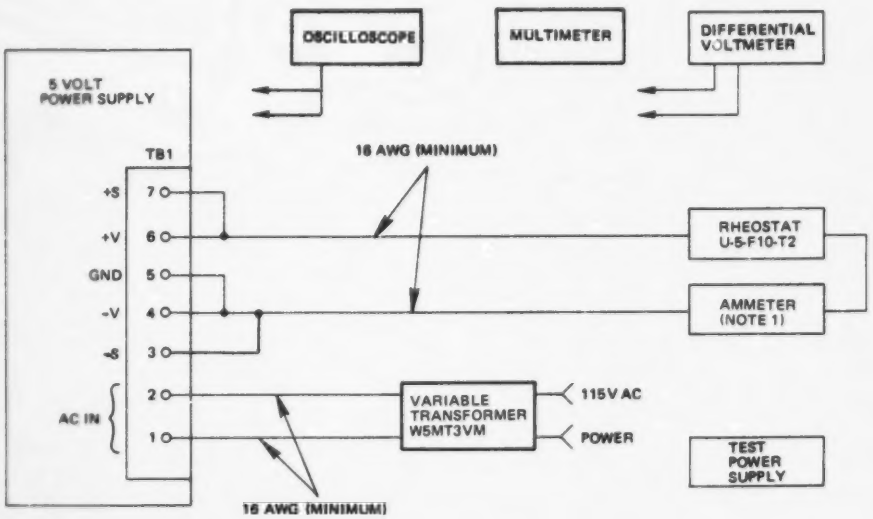
(e) Power rheostat, Ohmite, model U-5-F10-T2 (0-2.5/5 ohms, 2000 W).

(f) Variable transformer, General Radio W5MT3VM or equivalent.

(g) Power supply, Power Design 5005R or equivalent.

(4) *Troubleshooting procedures.* The troubleshooting procedures for the −5 V DC and +5 V DC power supplies are provided in tables 5-4 and 5-6, respectively. The location of parts within the −5 V DC and +5 V DC power supplies are shown in figures 5-2 and 5-3, respectively.

(5) *Test procedures.* The test procedures for the −5 V DC and +5 V DC power supplies are provided in tables 5-5 and 5-7, respectively.



NOTE:
1. MAKE SURE AMMETER IS SET AT CORRECT RANGE BEFORE APPLYING POWER.

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Figure 5-1. +5 V DC and −5 V DC Power Supply, Test Setup Diagram.

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Table 5-4. −5 V DC Power Supply, Troubleshooting Chart

Item no.	Malfunction	Probable cause	Corrective action
1	0.0 V dc output.	a. OUTPUT VOLTAGE control (R8) turned fully ccw.	a. Check OUTPUT VOLTAGE control (R8) for proper setting and correct as necessary.
		b. Short circuit across output of supply.	b. Check load and load connections, correct as necessary.
		c. Power transistor section open.	c. Check Q6 through Q9 and R25 through R28 for open. Replace as necessary.
		d. Series regulator section open.	d. Check Q1, Q2, and Q18. Replace as necessary.
		e. Current sensing resistor R25 open.	e. Check R25 for open, R6 for short.
		f. Aux rectifier CR1 open.	f. Check CR1 for open. Replace as necessary.
		g. Open CR8 or R1.	g. Check and replace as necessary.
		h. Full wave rectifier defective.	h. Check S1, CR2, CR3 and T1. Replace as necessary.
		i. Reference voltage section defective.	i. Check CR1 and IC1. Replace as necessary.
2	Unable to adjust voltage.	Damaged OUTPUT VOLTAGE control.	Check R8 for short or open, replace as necessary.
3	High ripple at line frequency or twice line frequency and unregulated dc output.	a. Series regulator transistors shorted.	a. Check and replace as necessary; Q1, Q2, Q6 through Q9.
		b. Defective main rectifier causes ripple at twice line frequency.	b. Check for open and/or short, CR2 and CR3.
		c. Defective drive rectifier.	c. Check for open and/or short, CR23 and CR24.
4	Same as 3, except intermittent.	Foreign matter fallen into unit.	Check for loose bench hardware and wire clippings that may have fallen through cover.
5	High ripple at frequency other than line or twice line frequency.	Oscillation due to defective component in filter network.	Check for open, C14 and C2, and check for open and/or short in C11 and R2. Replace defective component.
6	Large spikes at output.	Capacitor C15 or C16 open.	Replace C15 or C16.

Table 5-5. −5 V DC Power Supply, Test Procedures

Step No.	Test Procedure	Performance Standard	Normal Indication	Abnormal Indication
1	a. Connect test equipment as shown in figure 5-1. Set rheostat for 1 ohm.	a. None	a. Not applicable	a. Not applicable.
	b. Connect differential voltmeter from +V to −V terminals.	b. None	b. Not applicable	b. Not applicable.
	c. Turn on ac power. Adjust variable transformer output to 115 V ac. Adjust rheostat for 5.8 A on ammeter. If necessary, adjust VOLTAGE potentiometer R20 for 5 ±0.05 V dc on differential voltmeter.	c. 5 ±0.005 V dc, 5.8 A	c. Proceed to step 5.	c. Proceed to step 2.
2	using multimeter, measure voltage from CR15 anode (board terminal 18) to +V terminal	9.6 ±0.5 V dc	Check F1. Replace defective part and repeat step 1.	Proceed to step 3.
3	Using multimeter, measure voltage from CR15 anode to Q3 collector.	+7.2 ±0.5 V	Proceed to step 4.	Check S1, CR14, CR15 and T1. Replace defective part and repeat step 1.
4	Using multimeter, measure voltage from IC1-14 (+) to IC1-7 (−).	+28.2 ±2.0 V dc	Check Q1−Q4, SCR1, and CR28. Replace defective part and repeat step 1.	Check CR1, CR21, and IC1. Replace defective part and repeat step 1.
5	Using oscilloscope, measure ripple voltage from +V to −V terminal.	10 mV p-p or less	Proceed to step 6.	Check C7, C6, and C1. Replace defective part and repeat this step.

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Table 5-5. −5 V DC Power Supply, Test Procedures—Continued

Step No.	Test Procedure	Performance Standard	Normal Indication	Abnormal Indication
6	a. Turn off ac power Disconnect rheostat from output terminals.	a. None	a. Not applicable	a. Not applicable
	b. Connect differential voltmeter and test power supply across +V and −V output terminals.	b. None	b. Not applicable	b. Not applicable
	c. Increase output voltage of test power supply while observing differential voltmeter. Note highest reading before output drops to less than 1 V dc.	c. 6.6 ±0.2 V dc	c. Remove ac power. Disconnect test equipment. Test completed.	c. For serial No. prefix E. Check SCR1 and CR28. Replace defective part and repeat this step. For serial No. prefix F or above, replace HC1 and repeat this step.

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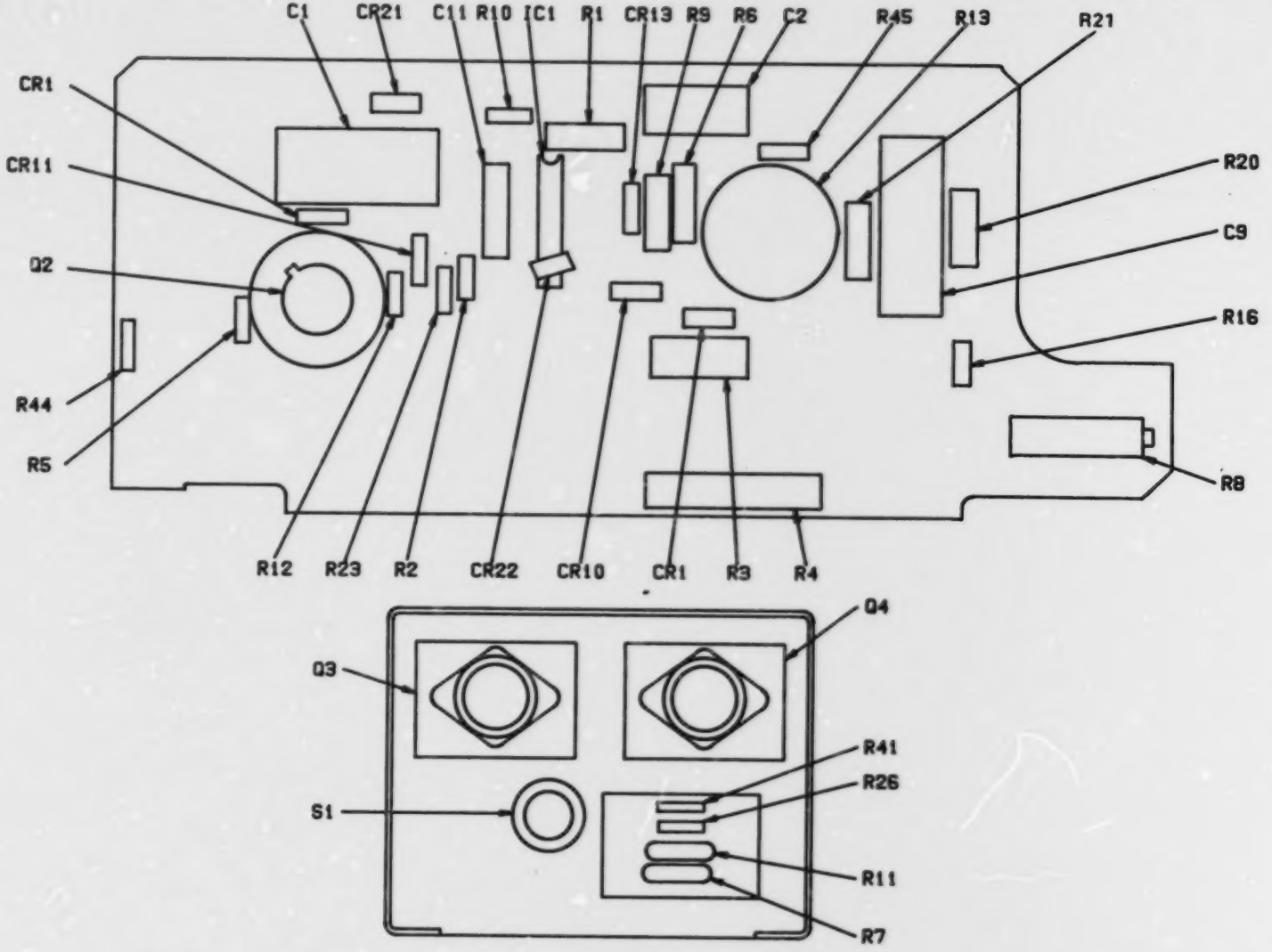

Figure 5-2 ①. −5 V DC Power Supply PS1, Parts Location Diagram (Sheet 1 of 2).

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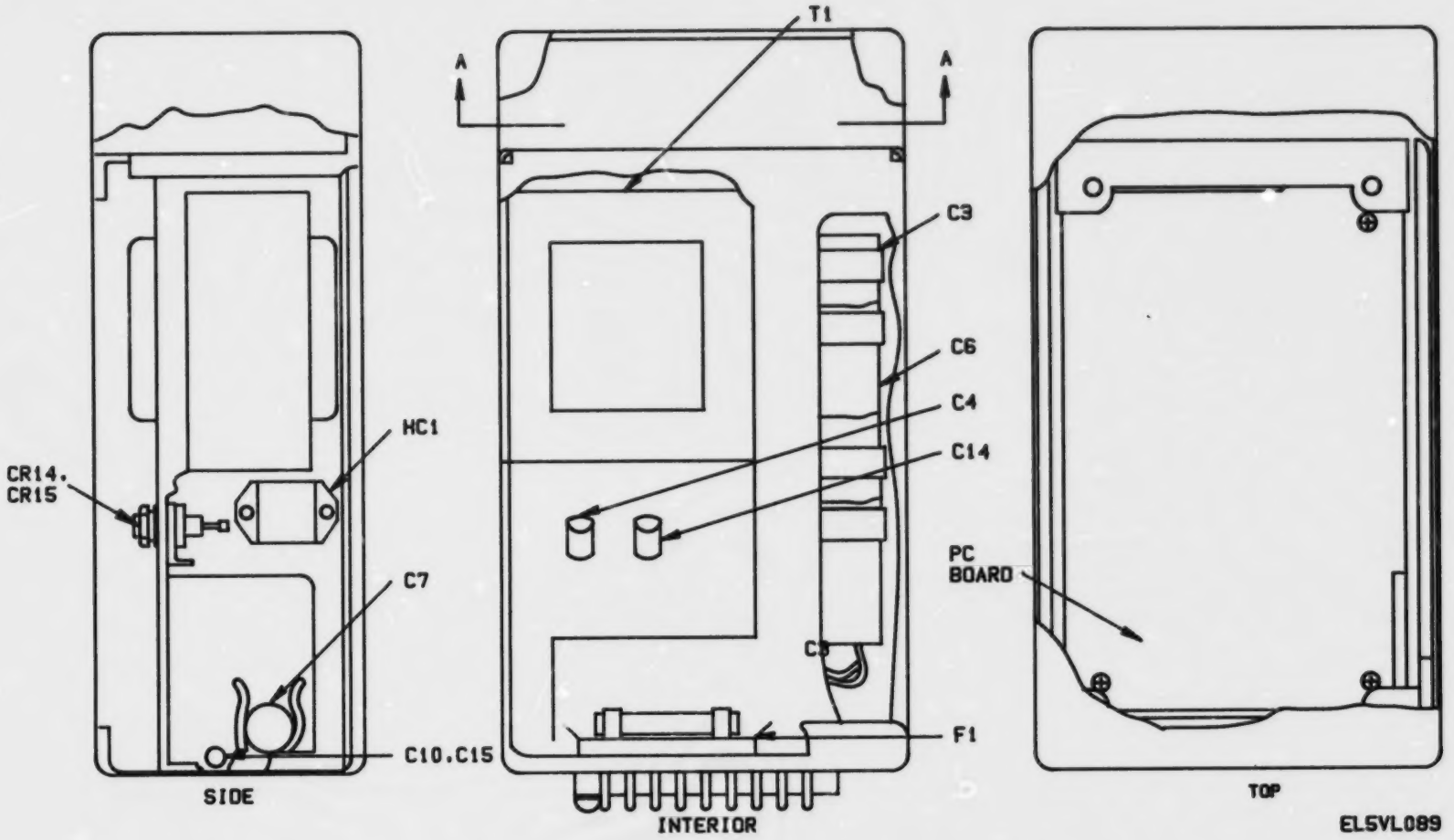

Figure 5-2②. −5 V DC Power Supply PS1, Parts Location Diagram (Sheet 2 of 2).

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Table 5-6. +5 V DC Power Supply, Troubleshooting Chart.

Item No.	Malfunction	Probable cause	Corrective action
1	0.0 V dc output.	*a.* OUTPUT VOLTAGE control (R8) turned fully ccw.	*a.* Check OUTPUT VOLTAGE control (R8) for proper setting and correct as necessary.
		b. Short circuit across output of supply.	*b.* Check load and load connections, correct as necessary.
		c. Fuse F1 open.	*c.* Replace F1; if it blows immediately, check shorted diode CR28, transistors Q1, Q2, Q3, and Q4, and capacitor C7; replace as necessary.
		d. Power transistor section open.	*d.* Check Q3 and Q4 for open, replace as necessary.
		e. Series regulator section open.	*e.* Check Q1 and Q2 for open, replace as necessary.
		f. Shorted CR28.	*f.* Check CR28 and replace as necessary.
		g. Current sensing resistor R7 open.	*g.* Check R7 for open, R6 for short.
		h. Aux rectifier CR1 open.	*h.* Check CR1 for open, replace as necessary.
		i. Open CR8 or R1.	*i.* Check and replace as necessary.
		j. Full wave rectifier defective.	*j.* Check S1, CR14, CR15, and T1. Replace as necessary.
		k. Reference voltage section defective.	*k.* Check CR1, CR21, and IC1. Replace as necessary.
2	Unable to adjust output voltage.	Damaged OUTPUT VOLTAGE control.	Check R8 for short and/or open, replace as necessary.
3	High ripple at line frequency or twice line frequency and unregulated dc output.	*a.* Series regulator transistors shorted.	*a.* Check and replace as necessary; Q1 through Q4.
		b. Defective main rectifier causes ripple at twice line frequency.	*b.* Check for open and/or short, CR14 and CR15.
4	Same as 3, except intermittent.	Foreign matter fallen into unit.	Check for loose bench hardware and wire clippings that may have fallen through cover.
5	High ripple at frequency other than line or twice line frequency.	Oscillation due to defective component in filter network.	Check for open, C7 and C2, and check for open and/or short in C11 and R2. Replace defective component.
6	Large spikes at output.	Capacitor C4 or C14 open.	Replace C4 or C14.

Table 5-7. +5 V DC Power Supply, Test Procedure.

Step No.	Test Procedure	Performance Standard	Normal Indication	Abnormal Indication
1	*a.* Connect test equipment as shown in figure 5-1. Set rheostat for 0.5 ohm.	*a.* None	*a.* Not applicable	*a.* Not applicable
	b. Connect differential voltmeter from +V to −V terminals.	*b.* None	*b.* Not applicable	*b.* Not applicable
	c. Turn on ac power. Adjust variable transformer output to 115 V ac. Adjust rheostat for 16A on ammeter. If necessary, adjust VOLTAGE potentiometer R8 for 5 ±0.05 V dc, on differential voltmeter.	*c.* 5 ±0.05 V dc, 16A	*c.* Proceed to step 5.	*c.* Proceed to step 2.
2	Using multimeter, measure voltage from Q7 collector to −V terminal.	+9.6 ±0.5 V dc	Proceed to step 3.	Check S1, CR2, CR3, and T1. Replace defective part and repeat step 1.
3.	Using multimeter, measure voltage from IC1-14(+) to IC1-7(−).	+25.2 ±2.0 V dc Proceed to step 4.	Proceed to step 4.	Check CR1 and IC1. Replace defective part and repeat step 1.
4	Using multimeter, measure voltage from CR23 cathode (1) to −V terminal.	+10 ±0.5 V dc	Check Q6—Q9, Q1, Q2, Q18 and HC1. Replace defective part and repeat step 1.	Check CR23 and CR24. Replace defective part and repeat step 1.

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Table 5-7. +5 V DC Power Supply Test Procedure—Continued.

Step No.	Test Procedure	Normal Indication	Abnormal Indication	
5	Using oscilloscope, measure ripple voltage from +V to −V terminals.	10 mV p-p or less.	Proceed to step 6.	Check C6, C14, C1 and C34. Replace defective part and repeat this step.
6	*a.* Turn off ac power. Disconnect rheostat from output terminals.	*a.* None	*a.* Not applicable.	*a.* Not applicable
	b. Connect differential voltmeter and test power supply across +V and −V output terminals.	*b.* None	*b.* Not applicable	*b.* Not applicable
	c. Increase output voltage of test power supply while observing differential voltmeter. Note highest reading before output drops to less than 1 V dc.	*c.* 6.6 ±0.2 V dc	*c.* Remove ac power.	*c.* Replace HC1 and repeat this step.

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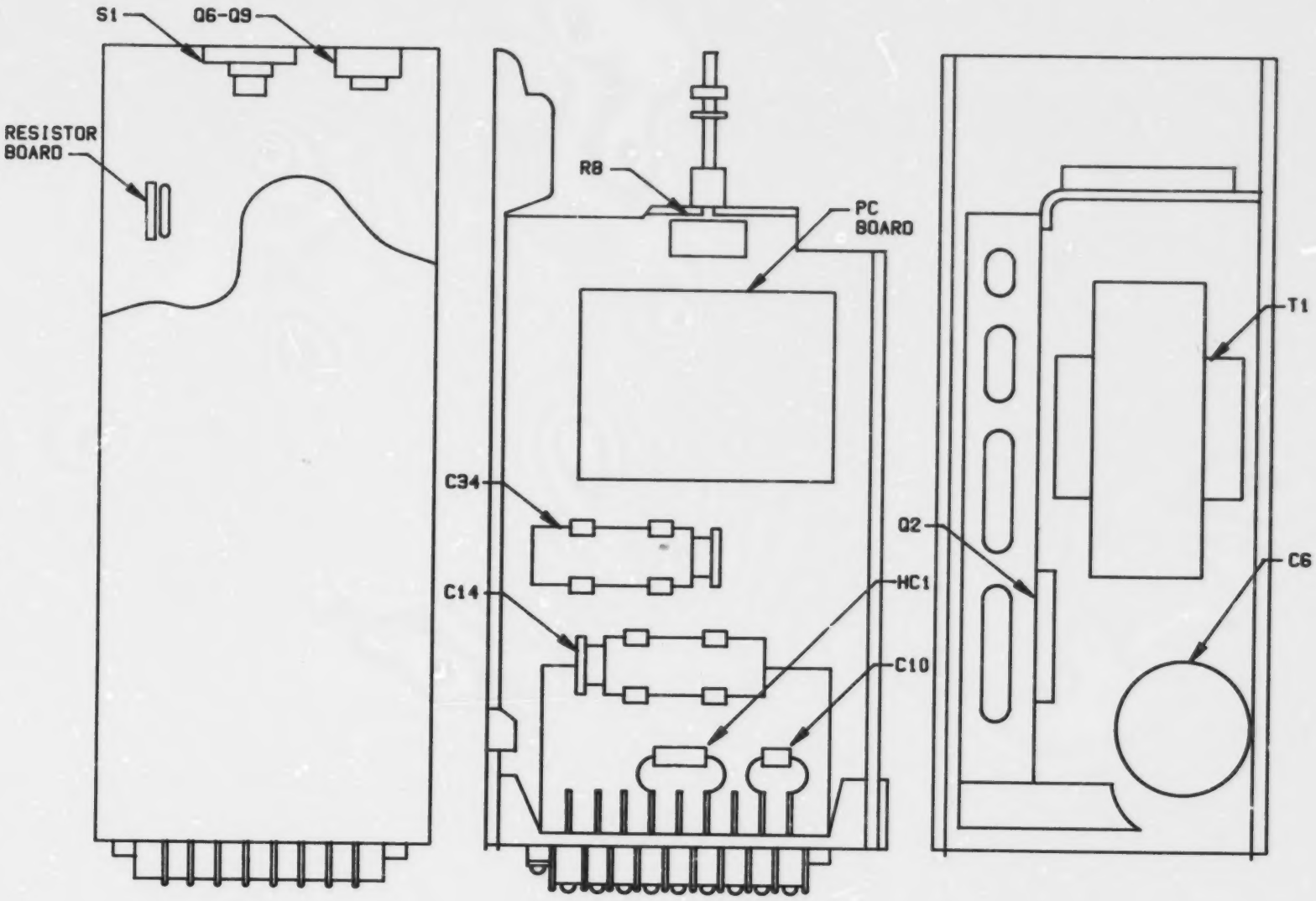

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Figure 5-3 ①. +5 V DC Power Supply PS2, Parts Location Diagram (Sheet 1 of 2).

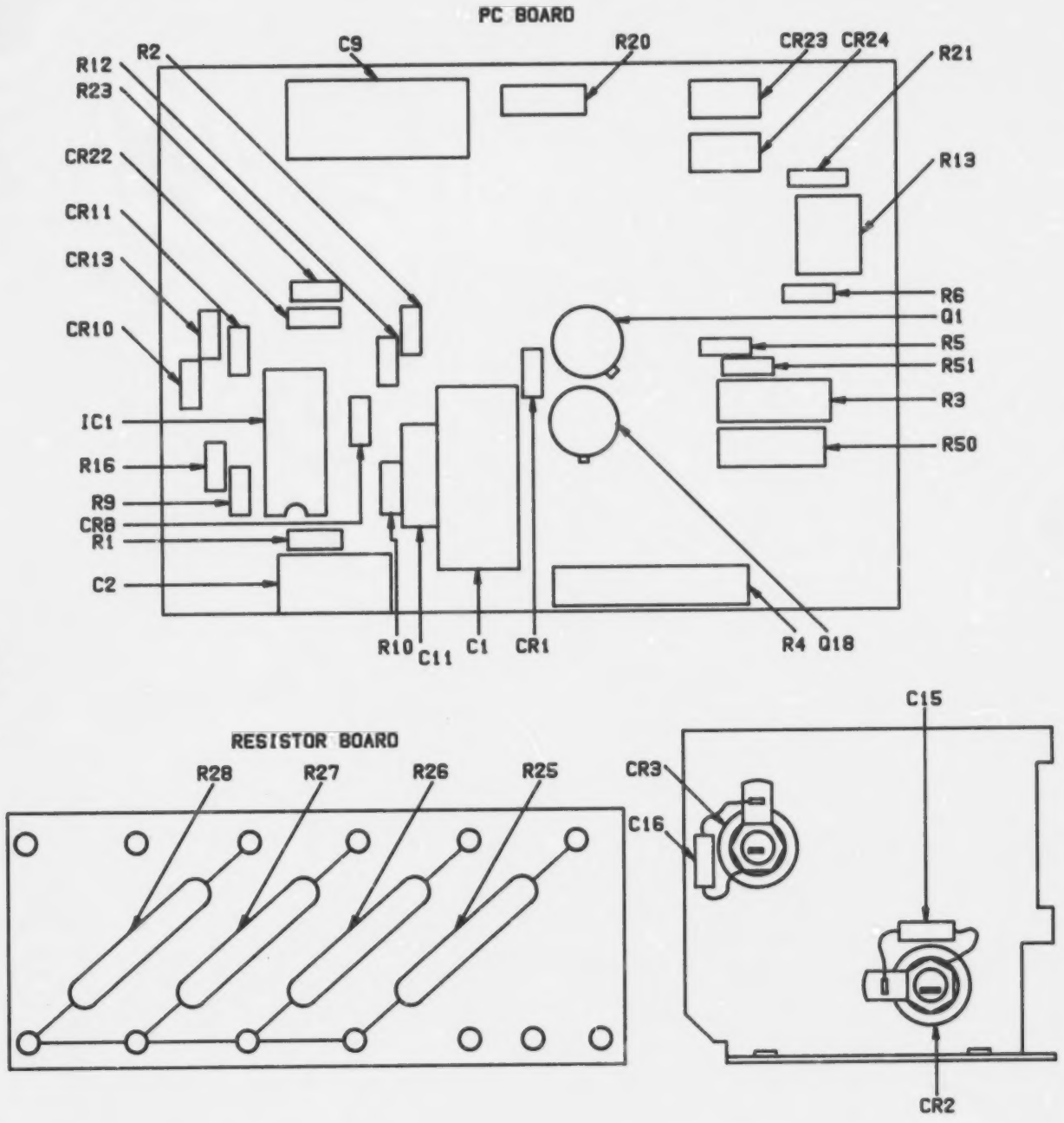

Figure 5-3 (2). +5 V DC Power Supply PS2, Parts Location Diagram (Sheet 2 of 2).

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d. Power Supply Controller Troubleshooting and Test. Refer to TM 11-5895-552-15/1, TM 11-5895-552-15/2, and TM 11-5895-552-15/3 for troubleshooting, test procedures, and location of parts for the power supply controller.

e. +16 V DC and −10 V DC Power Supply Troubleshooting and Test. Refer to TM 11-5895-552-15/1, TM 11-5895-552-15/2, and TM 11-5895-552-15/3 for troubleshooting, test procedures, and location of parts for the +16 V DC and −10 V DC power supplies.

5-7. Adjustment Procedures

a. General. The following paragraphs provide adjustment procedures for the −5 V DC and +5 V DC power supplies. These adjustments are required infrequently and they should not be performed unless critical parts are replaced in the power supplies.

b. Test Equipment. Refer to paragraph 5-6c(3) for test equipment required to adjust the −5 V DC and +5 V DC power supplies. The test equipment setup is shown in figure 5-1.

c. −5 V DC Power Supply Calibration Control (R13) Adjustment. Whenever Q3, Q4, R6, R7, R9, R11, R13, R21, or IC1 are replaced, and voltage and current indications do not reflect maximum ratings, adjust R13 before replacing the power supply cover. The adjustment procedure requires that the power supply is removed from the SSCC, is at an ambient temperature of +77 to +85° F, and is stabilized. Adjust calibration control R13 as follows:

(1) Remove ac input power from the module.

(2) Break the seal on the wiper of R13 to free it from the resistor housing, and turn fully clockwise.

(3) Operate module for constant voltage with the power rheostat and local sensing connected as shown in figure 5-1.

(4) Adjust the variable transformer to provide an input of 115 V ac to the power supply.

(5) Turn voltage adjust control until the power supply output is 4.75 V dc.

(6) Adjust the power rheostat so that the power supply output current is 6.38 amperes.

(7) Using the oscilloscope, observe the output ripple voltage while adjusting R13 counterclockwise. Adjust R13 until output ripple begins to increase.

(8) Turn voltage adjust control until the power supply output is 5.25 V dc.

(9) Increase the power supply load. Maximum attainable load current shall not exceed 7.54 amperes.

(10) After the adjustment is completed, remove ac power input from the power supply and reseal the wiper of R13 to the resistor housing using Glyptal (para 5-2*b*(7)).

(11) After sealing the wiper of R13, check its setting. Repeat the adjustment procedure, if required.

(12) Perform applicable checks in table 5-5.

d. +5 V DC Power Supply Calibration Control (R13) Adjustment. Whenever Q6 through Q9, R6, R25 through R28, R9, R13, R21, or IC1 is replaced and voltage and current indications do not reflect maximum ratings, adjust R13 before replacing the power supply cover. The adjustment procedure requires that the power supply is removed from the SSCC, is at an ambient temperature of +77 to +85° F, and is stabilized. Adjust calibration control R13 as follows:

(1) Remove ac input power from the module.

(2) Break the seal on the wiper of R13 to free it from the resistor housing, and turn fully clockwise.

(3) Operate module for constant voltage with the power rheostat and local sensing connected as shown in figure 5-1.

(4) Adjust the variable transformer to provide an input of 115 V ac to the power supply.

(5) Turn voltage adjust control until the power supply output is 4.75 V dc.

(6) Adjust the power rheostat so that the power supply output current is 17.6 amperes.

(7) Using the oscilloscope, observe the output ripple voltage while adjusting R13 counterclockwise. Adjust R13 until output ripple begins to increase.

(8) Turn voltage adjust control until the power supply output is 5.25 V dc.

(9) Increase the power supply load. Maximum attainable module load current shall not exceed 20.8 amperes.

(10) After the adjustment is completed, remove ac power input from the power supply and reseal the wiper of R13 to the resistor housing using Glyptal (para 5-2*b*(7)).

(11) After sealing the wiper of R13, check its setting. Repeat the adjustment procedure, if required.

(12) Perform applicable checks in table 5-7.

e. +16 VDC and −10 V DC Power Supply Adjustment. Refer to TM 11-5895-552-15/1, TM 11-5895-552-15/2, and TM 11-5895-552-15/3 for adjustment procedures and location of parts for the +16 V DC and −10 V DC power supplies.

5-8. Removal and Replacement

a. General. The following paragraphs provide step-by-step procedures for removal and replacement of SSCC components.

NOTE

All indicator and switch lamps on the console panel are type 330 incandescent lamps.

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b. Processor Panel Register and Status Indicator Removal and Replacement.

(1) *Indicator lamp (fig. FO-3).*

(a) Unscrew the indicator lamp lens on front panel.

(b) Remove the defective lamp from the rear of the indicator lens.

(c) Replace the defective lamp with one that is known to the good.

(d) Screw the indicator lamp lens on front panel.

(2) *Indicator socket assembly (fig. FO-3 and FO-5).*

CAUTION

Remove power from the SSCC before attempting removal of any indicator socket assembly.

(a) Open the hinged front panel as far as possible.

(b) Tag and remove the two leads to the indicator socket assembly.

(c) At the rear of the front panel, remove the nut and washer which secure the indicator socket assembly to the front panel.

(d) Remove the indicator socket assembly from the front panel.

(e) Replace the defective socket assembly with one that is known to be good.

(f) Complete the replacement procedure by reversing the removal procedure in *(a)*, *(b)* and *(c)* above.

c. Processor Panel T and KA Rocker Switch Removal and Replacement (fig. FO-3 and FO-5).

CAUTION

Remove power from the SSCC before attempting removal of a rocker switch from the processor panel.

(1) Open the hinged front panel as far as possible.

(2) Tag and remove all leads connected to the rocker switches. (For rocker switches S1 through S32 and S34 through S49, the entire block of switches must be replaced when any switch within a block is defective.)

(3) For rocker switches S66 and S67, remove the two nuts and washers which secure the rocker switch to the panel.

(4) For rocker switches S1 through S32 and S34 through S49, remove the six washers and nuts which secure the applicable supporting strips to the panel and remove the supporting strips.

(5) Remove the rocker switches from the panel.

(6) Replace each defective rocker switch and each defective block with a unit that is known to be good.

(7) Complete the replacement procedure by reversing the removal procedure in (1) through (5) above.

d. Processor Panel Tape Switch/Indicator Removal and Replacement.

(1) *Indicator lamp (fig. FO-3).*

(a) Remove plastic indicator by pulling it straight out from the panel.

(b) Pull miniature bulbs from its socket in plastic indicator.

(c) Replace bulbs with one that is known to be good.

CAUTION

Do not use excessive force when reinserting plastic indicator. If indicator will not snap easily into place, rotate it 180° and try again.

(d) Reinsert plastic indicator and snap into place.

(2) *Switch assembly (fig. FO-3 and FO-5).*

CAUTION

Remove power to the SSCC before attempting removal of a switch assembly.

(a) Open the hinged front panel as far as possible.

(b) Tag and remove all leads connected to the switch assembly.

(c) Close the hinged front panel.

(d) Remove the plastic indicator as directed in (1) above.

(e) Loosen the two spring-held screws within the switch assembly (upper right and lower left corners as viewed from the front) until the associated holding clips are released.

(f) Remove the switch assembly from the front panel.

(g) Reinsert a switch assembly that is known to be good into the vacated switch location.

(h) Push the two holding clips out so that they secure the switch assembly to the panel; tighten the two spring-held screws.

(i) Complete the replacement procedure by reversing the removal procedures in *(a)* and *(b)* above.

e. Processor Panel Control Switch/Indicator.

(1) *Indicator lamp (fig. FO-3).*

(a) Remove plastic indicator by pulling it straight out from panel.

(b) Pull miniature bulbs from its socket in plastic indicator.

(c) Replace bulbs with one that is known to be good.

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CAUTION

Do not use excessive force when reinserting plastic indicator. If indicator will not easily snap into place, rotate it 180° and try again.

(d) Reinsert plastic indicator into position and snap into place.

(2) *Switch or switch/indicator assembly (fig. FO-3 and FO-5).*

CAUTION

Remove power to the SSCC before attempting to remove a switch or switch/indicator assembly.

(a) Open the hinged front panel as far as possible.

(b) Tag and remove all leads connected to the switch or switch/indicator assembly.

(c) Remove the assembly by depressing the spring holders and pushing the assembly out through the front panel.

(d) Insert a replacement component which is known to be good into the vacated hole (from the front) and snap into place.

(e) Reconnect all leads to their proper terminals.

(f) Close the hinged front panel.

f. Plug-in Circuit Card Removal and Replacement.

(1) The location of specific printed-circuit cards by pan level and location is shown in the applicable logic diagrams (drawings 9L08674 and 9L08948). For the location of parts on the printed-circuit cards, refer to the placement chart in the logic diagrams for the SSCC.

(2) No special procedures are required for removing and replacing printed-circuit cards, other than observation of the following precautions:

(a) After opening respective logic page for printed circuit card exposure, use a card puller for printed circuit card removal.

(b) During maintenance when testing of a printed-circuit card is required, do not use probes with the printed-circuit card fully seated in its slot. Use the card extender to provide adequate access for connecting the probes.

CAUTION

Do not apply an external voltage to a test point other than a voltage which might be prescribed in the applicable test procedures. Extreme care should be exercised when performing resistance measurements on transistorized circuits. Transistors may become damaged.

(c) When replacing printed-circuit cards, be sure to insert them in their proper slots. The module placement diagram within the logic diagram set lists the card number, and shows the card location and mating slot number.

CAUTION

It is possible to insert a card in the wrong slot. If this happens, considerable damage is likely to result.

(d) When installing a printed-circuit module, gently aline it with receptacle and with guide pins on connector. Firmly push the module in place until it is seated. Double-check to see that the installed module is not misalined.

(e) When replacing a printed-circuit module, check to see that the type of module being replaced is the required type.

g. Power Supply Controller Removal and Replacement.

(1) *Removal.* Procedures for removing the power supply controller (refer to fig. 5-4 are as follows:

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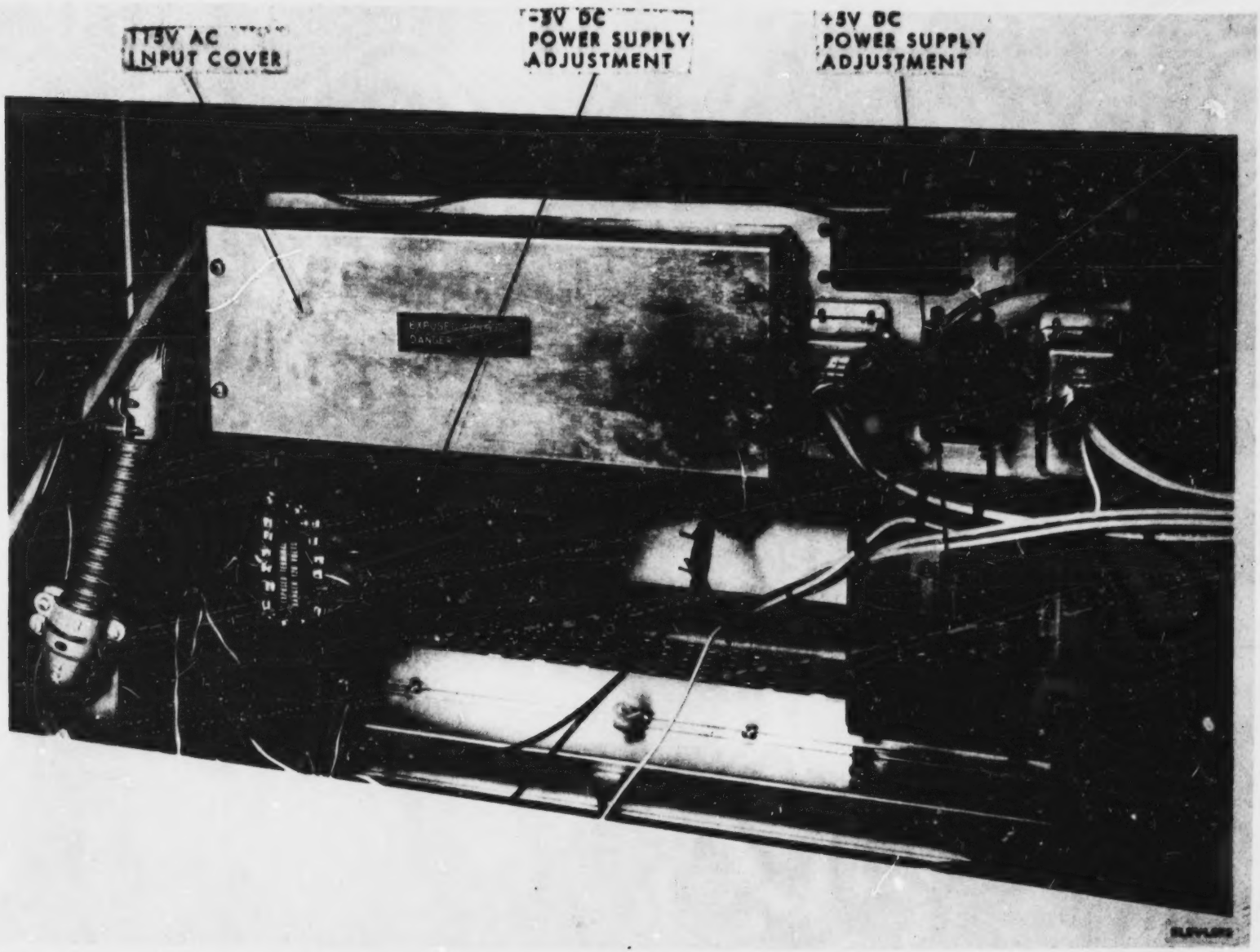

Figure 5-4 ①. Power Supply Controller, Removal and Replacement (Sheet 1 of 2).

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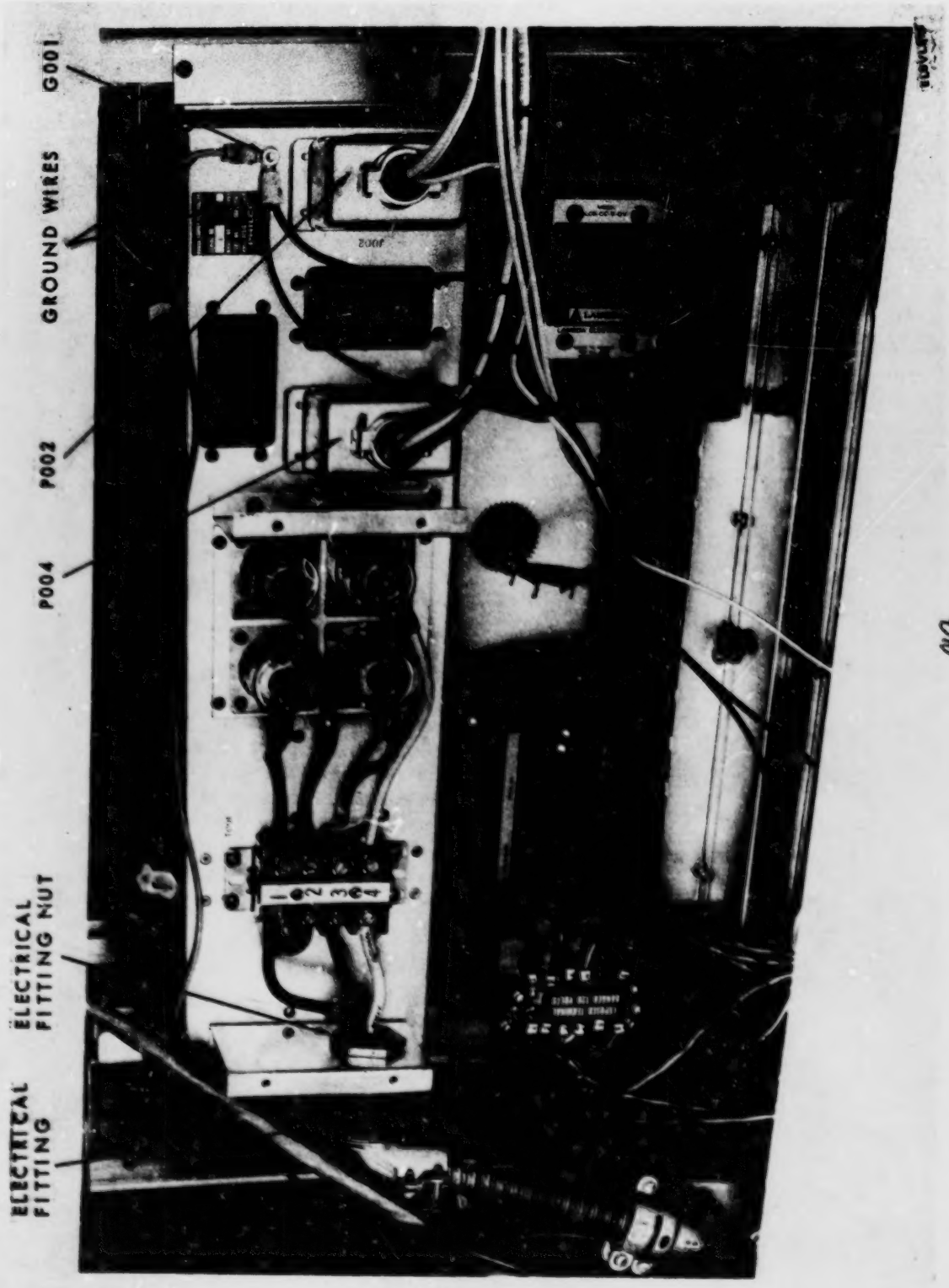

Figure 5-4①. Power Supply Controller, Removal and Replacement (Sheet 2 of 2).

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CAUTION

Make certain that all primary ac power is disconnected from the power supply controller. This is accomplished by setting the main SSCC power circuit breaker to off.

(a) Remove four screws and 115 V ac input cover.

(b) Remove electrical fitting nut. Disconnect conduit and electrical fitting from power supply controller.

(c) Disconnect P002 nd P004.

(d) Remove green ground wires connected to G001.

(e) Remove four screws from power supply controller front panel.

WARNING

The power supply controller is extremely heavy. Do not perform the remainder of the procedure alone. A minimum of two people should be used to remove the unit from the console.

(f) With one person at each side, slowly withdraw the power supply controller from the console. Be careful to provide sufficient lift while withdrawing unit to prevent unit from tipping over or becoming misalined with guide rails.

(g) Gently lower unit to a suitable height and place it on a work table or transportation dolly.

(2) *Replacement.* Replace the power supply controller in the reverse order of the procedures given above. Refer to figure 5-4.

h. +16 V DC, −10 V DC and −27 V DC Power Supplies, Removal and Replacement.

(1) *Removal.* Procedures for removing any of the power supplies are as follows:

WARNING

Make certain that all primary ac power is disconnected from the equipment and that all front panel power switches are turned off.

(a) Remove rear door of applicable equipment cabinet bay, containing the power supply to be removed (see fig. 1-6 for power supply locations), in accordance with *j* below.

(b) Remove all screws, securing insulating cover to studs. Cover will hang freely on beaded chain.

(c) Remove screw, retaining insulating cover to beaded chain.

(d) Tag all leads to output terminals and terminal boards which are routed from elsewhere within the equipment cabinet.

(e) Remove screws and loosen cable clamp from power supply front panel. Remove tagged leads from output terminals and terminal strips. Dress wires away from power supply front panel.

(f) Remove screws, lockwashers, and flat washers, securing power supply front panel (two screws at either side) to equipment frame within cabinet.

WARNING

The power supply is extremely heavy. Do not perform the remainder of the procedure alone. A minimum of two people should be used to remove the power supply from the cabinet.

(g) With one person at either side at rear of equipment cabinet, slowly withdraw power supply from cabinet. Be careful to provide sufficient lift while withdrawing power supply, so that unit will not tip or become misalined with guide rails.

(h) Gently lower unit to a suitable height and place it on a work table or transportation dolly.

(2) *Replacement.* Replace the power supply in the reverse order of the procedure given in (1) above.

i. +5 V DC and −5 V DC Power Supplies, Removal and Replacement.

(1) *Removal.* Procedures for removing either power supply are given below:

WARNING

Make certain that all primary ac power is disconnected from the power supplies. This is accomplished by pressing the power supply controller panel red STOP switch and then setting the three ac power circuit breakers to off.

(a) Remove four screws securing insulating cover to studs.

(b) Tap all leads connected to power supply output terminals.

(c) While a second person is holding the power supply from the front, unscrew the four standoff posts and remove power supply.

(2) *Replacement.* Replace the power supply in the reverse order of the removal.

j. Equipment Cabinet Door Removal and Replacement.

(1) *Removal.* Remove the equipment cabinet doors as follows:

(a) Open the door (front or rear) until it makes an angle of approximately 45° with the cabinet frame.

(b) At the bottom point of attachment, grasp the free end of the slotted door-stop bracket and pull upward, disengaging it from the stationary stud.

(c) At the top of attachment on the door, pull down the spring-loaded L-shaped latch to release the door from the frame.

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(d) Move the door outward from the cabinet until the latch pin is clear of the frame. Release latch.

(e) Lift door, disengaging pin from the hole in the cabinet frame, thus freeing the door from the cabinet.

(2) *Replacement.*

(a) With the door held in the wide-open position, insert pin at the bottom corner of door into the hole in the cabinet frame.

(b) At top of the door, pull down the spring-loaded latch and then release it to engage the hole in the cabinet frame.

(c) Position the door so that it makes an angle of 45° with the cabinet frame.

(d) At the bottom point of attachment, place the door-stop slotted bracket over the stationary stud.

(e) Engage slotted bracket over the stationary stud, and secure by pressing downward on the free end of the slotted bracket.

k. Door Gasket. The rubber door gasket around the inside frame, insulating each bay of the maintenance console, is secured to the frame with a series of spring clips. Remove the gasket from the frame by inserting a screwdriver behind the rubber gasket and prying out the clips. When replacing the door gasket, aline the gasket around the door frame and slide the spring clips in place.

l. Cabinet Blower Assembly. Removal instructions for a cabinet blower assembly are given below. Replacement of the cabinet blower is the reverse of removal.

(1) Open rear door of equipment cabinet. Make certain that all primary ac power is disconnected from the equipment cabinet, and that all power supply and power supply controller front panel switches are off (para 3-5).

(2) Disconnect power connector (front of bay) from blower assembly at bottom of equipment cabinet.

(3) Remove six screws, lockwashers, and flat washers, securing mounting plate of blower assembly to bottom frame of equipment cabinet.

(4) Carefully lift out blower assembly.

m. Clock Panel Removal and Replacement.

(1) *Removal.* Procedures for removing the clock panel are given below:

WARNING

Make certain that all primary ac power is disconnected from the clock panel. This is accomplished by pressing the power supply controller panel STOP switch and then setting the three ac power circuit breakers to off.

(a) Tag leads and disconnect them from the terminal board.

(b) Remove four front panel screws. Remove clock panel.

(2) *Replacement.* Replace the clock panel in the reverse order of the removal.

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APPENDIX A

REFERENCES

The following publications contain information applicable to the operation and maintenance of the OJ-50/FYA-10(V).

DA PAM 310-1	Consolidated Index of Army Publications and Blank Forms.
DA Pam 738-750	The Army Maintenance Management Systems (TAMMS).
DCA310-D70	DCS AUTODIN General Description.
DCA310-D70-32	DCS AUTODIN Supervisory Commands and Printouts.
DCAC310-D70-35	DCS AUTODIN Data Dictionary.
DCAC310-D70-36	DCS AUTODIN Description of the Test and Diagnostic Program.
DCAC310-D70-41	DCS AUTODIN Utility Programs.
SB 38-100	Preservation, Packaging, Packing and Marking Materials, Supplies and Equipment Used by the Army.
TB 43-0118	Field Instructions for Painting and Preserving Electronics Command Equipment Including Camouflage Pattern Painting of Electrical Equipment Shelters.
TB SIG 222	Solder and Soldering.
TB SIG 355-1	Depot Inspection Standard for Repaired Signal Equipment.
TB SIG 355-2	Depot Inspection Standard for Refinishing Repaired Signal Equipment.
TB SIG 355-3	Depot Inspection Standard for Moisture and Fungus Resistant Treatment.
TM 11-5895-391-15	Operator, Organizational, Direct Support, General Support, and Depot Maintenance Manual: Automatic Digital Message Switching Centers AN/FYQ-42(V)1 Through AN/FYQ-42(V)12 and AN/FYQ-42(V)T1.
TM 11-5895-402-15/1	Operator's Organizational, Direct Support, General Support, and Depot Maintenance Manual: Printed Circuits for Automatic Digital Message Switching Groups AN/FYA-10(V)1 through AN/FYA-10(V) 7 and AN/FYA-10(V)T1.
TM 11-5895-402-15/2	Operator's Organizational, Direct Support, General Support, and Depot Maintenance Manual: Printed Circuits for Automatic Digital Message Switching Groups AN/FYA-10(V)1 Through AN/FYA-10(V)7 and AN/FYA-10(V)T1.
TM 11-5895-406-15/1	Operator's, Organizational, Direct Support, General Support, and Depot Maintenance Manual: Processor Unit OL-9/FYA-10(V).
TM 11-5895-406-15/2	Operator's Organizational, Direct Support, General Support, and Depot Maintenance Manual: Processor Unit OL-9/FYA-10(V).
TM 11-5895-416-14	Operator's Organizational, Direct Support, and General Support Maintenance Manual: Intercommunication Sets AN/FYA-39 and AN/FYA-55.
TM 11-5895-554-15/1	Operator's Organizational, Direct Support, General Support, and Depot Maintenance Manual: Printed Circuit Card Tester for Automatic Digital Message Switching Groups AN/FYA-10(V)1 through AN/FYA-10(V)7 and AN/FYA-10(V)T1.
TM 11-5895-554	Operator's Organizational, Direct Support, General Support and Depot Maintenance Manual: Printed Circuit Card Tester for Automatic Digital Message Switching Groups AN/FYA-10(V)1 through AN/FYA-10(V)7 and AN/FYA-10(V)T1.
TM 11-5895-554-15/3	Operator's Organizational, Direct Support, Depot Maintenance Manual: Printed Circuit Card Tester for Automatic Digital Message Switching Groups AN/FYA-10(V)1 through AN/FYA-10(V)7 and AN/FYA-10(V)T1.
TM 11-5895-747-15/1	Operator's Organizational, DS, GS, and Depot Maintenance Manual: Data and Wiring List, Automatic Digital Message Switching Groups AN/FYA-10(V)1 Through AN/FYA-10(V)7 and AN/FYA-10(V)T1 of Automatic Digital Message Switching Centers AN/FYQ-42(V)1 through AN/FYQ-42(V)12 and AN/FYQ-42(V)T1 (Part I of II); AN/FYA-10(V)1 through AN/FYA-10(V)7 and AN]FYA-10(V)T1.

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TM 11-5895-747-15/2	Operator's Organizational, DS, GS, and Depot Maintenance Manual: Data and Wiring List for Automatic Digital Message Switching Groups AN/FYA-10(V)1 through AN/FYA-10(V)7 and AN/FYA-10(V)T1 of Automatic Digital Message Switching Centers AN/FYQ-42(V)1 through AN/FYQ-42(V)12 and AN/FYQ-42(V)T1 (Part II of II), AN/FYA-10(V)1 through AN/FYA-10(V)7 and AN/FYA-10(V)T1.
TM 11-5895-839-14	Operator's Organizational, Direct Support, and General Support Maintenance Manual: Console, Message OJ-347/FYA-10(V) (NSN 5895-01-016-2679).
TM 11-5895-1094-14	Operator's, Organizational, Direct Support, and General Support Maintenance Manual: Digital Data Terminal AN/FYQ-89.

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APPENDIX D

MAINTENANCE ALLOCATION

Section I. INTRODUCTION

D-1. General

This appendix provides a summary of the maintenance operations for OJ-50/FYA-10(V). It authorizes categories of maintenance for specific maintenance functions on repairable items and components and the tools and equipment required to perform each function. This appendix may be used as an aid in planning maintenance operations.

D-2. Maintenance Function

Maintenance functions will be limited to and defined as follows:

a. Inspect. To determine the serviceability of an item by comparing its physical, mechanical, and/or electrical characteristics with established standards through examination.

b. Test. To verify serviceability and to detect incipient failure by measuring the mechanical or electrical characteristics of an item and comparing those characteristics with prescribed standards.

c. Service. Operations required periodically to keep an item in proper operating condition, i.e., to clean (decontaminate), to preserve, to drain, to paint, or to replenish fuel, lubricants, hydraulic fluids, or compressed air supplies.

d. Adjust. To maintain, within prescribed limits, by bringing into proper or exact position, or by setting the operating characteristics to the specified parameters.

e. Align. To adjust specified variable elements of an item to bring about optimum or desired performance.

f. Calibrate. To determine and cause corrections to be made or to be adjusted on instruments or test measuring and diagnostic equipments used in precision measurement. Consists of comparisons of two instruments, one of which is a certified standard of known accuracy, to detect and adjust any discrepancy in the accuracy of the instrument being compared.

g. Install. The act of emplacing, seating, or fixing into position an item, part, module (component or assembly) in a manner to allow the proper functioning of the equipment or system.

h. Replace. The act of substituting a serviceable like type part, subassembly, or module (component or assembly) for an unserviceable counterpart.

i. Repair. The application of maintenance services (inspect, test, service, adjust, align, calibrate, replace) or other maintenance actions (welding, grinding, riveting, straightening, facing, remachining, or resurfacing) to restore serviceability to an item by correcting specific damage, fault, malfunction, or failure in a part, subassembly, module (component or assembly), end item, or system.

j. Overhaul. That maintenance effort (service/action) necessary to restore an item to a completely serviceable/operational condition as prescribed by maintenance standards (i.e., DMWR) in appropriate technical publications. Overhaul is normally the highest degree of maintenance performed by the Army. Overhaul does not normally return an item to like new condition.

k. Rebuild. Consists of those services/actions necessary for the restoration of unserviceable equipment to a like new condition in accordance with original manufacturing standards. Rebuild is the highest degree of materiel maintenance applied to Army equipment. The rebuild operation includes the act of returning to zero those age measurements (hours, miles, etc.) considered in classifying Army equipments/components.

D-3. Column Entries

a. Column 1, Group Number. Column 1 lists group numbers, the purpose of which is to identify components, assemblies, subassemblies, and modules with the next higher assembly.

b. Column 2, Component/Assembly. Column 2 contains the noun names of components, assemblies, subassemblies, and modules for which maintenance is authorized.

c. Column 3, Maintenance Functions. Column 3 lists the functions to be performed on the item listed in column 2. When items are listed without maintenance functions, it is solely for purpose of having the group numbers in the MAC and RPSTL coincide.

d. Column 4, Maintenance Category. Column 4 specifies, by the listing of a "work time" figure in the appropriate subcolumn(s), the lowest level of maintenance authorized to perform the function listed in column 3. This figure represents the active time required to perform that maintenance function at the indicated category of maintenance. If the number or

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complexity of the tasks within the listed maintenance function vary at different maintenance categories, appropriate "work time" figures will be shown for each category. The number of task-hours specified by the "work time" figure represents the average time required to restore an item (assembly, subassembly, component, module, end item or system) to a serviceable condition under typical field operating conditions. This time includes preparation time, troubleshooting time, and quality assurance/quality control time in addition to the time required to perform the specific tasks identified for the maintenance functions authorized in the maintenance allocation chart. Subcolumns of column 4 are as follows:

C-Operator/Crew
O-Organizational
F-Direct Support
H-General Support
D-Depot

e. Column 5, Tools and Equipment. Column 5 specifies by code, those common tool sets (not individual tools) and special tools, test, and support equipment required to perform the designated function.

f. Column 6, Remarks. Column 6 contains an alphabetic code which leads to the remark in section IV, Remarks, which is pertinent to the item opposite the particular code.

D-4. Tool and Test Equipment Requirements (Sect. III)

a. Tool or Test Equipment Reference Code. The numbers in this column coincide with the numbers used in the tools and equipment column of the MAC. The numbers indicate the applicable tool or test equipment for the maintenance functions.

b. Maintenance Category. The codes in this column indicate the maintenance category allocated the tool or test equipment.

c. Nomenclature. This column lists the noun name and nomenclature of the tools and test equipment required to perform the maintenance functions.

d. National/NATO Stock Number. This column lists the National/NATO stock number of the specific tool or test equipment.

e. Tool Number. This column lists the manufacturer's part number of the tool followed by the Federal Supply Code for manufacturers (5-digit) in parentheses.

D-5. Remarks (Sect. IV)

a. Reference Code. This code refers to the appropriate item in section II, column 6.

b. Remarks. This column provides the required explanatory information necessary to clarify items appearing in section II.

(Next printed page is D-3)

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SECTION II MAINTENANCE ALLOCATION CHART
FOR

CONSOLE, SYSTEM STATUS CONTROL OJ-50/FYA-10(V)

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT.	(6) REMARKS
			C	O	F	H	D		
00	CONSOLE, SYSTEM STATUS CONTROL OJ-50/FYA-10(V)	Inspect				0.2		1	A
		Service				0.2		32	B
		Test				0.5		2,4,7	C,D
		Adjust				0.5		3,5	E
		Repair				2.0		1	F,G
		Overhaul					80.0	1 thru 31	
01	PROCESSOR ASSEMBLY, A1 398-7737-1	Repair				0.4		1	F
0101	CABINET ASSEMBLY 398-7740-1	Service				0.2		32	B,I
010101	BLOWER ASSEMBLY KBB-32-32-2	Replace				0.5		1	
		Repair				0.8		1	
0102	PROCESSOR PANEL NO. 1 398-7438-3	Test				0.5		1,4,5	D,H
		Repair				0.3		1	G
010201	CIRCUIT CARD ASSEMBLY, CON 12C 398-7157-3	Test				0.3		2	
		Replace				0.5		1	
		Repair				0.2		1	
010202	CIRCUIT CARD ASSEMBLY, CON 12E 398-7157-5								K
010203	CIRCUIT CARD ASSEMBLY, CON 12G 398-7157-7								K
010204	CIRCUIT CARD ASSEMBLY, CON 13A 398-7206-1								K
010205	CIRCUIT CARD ASSEMBLY, CON 6F 398-4350-7	Replace				0.5		1	
0103	FUNCTIONAL ASSEMBLY, PROCESSOR 398-7507-2	Test				1.0		2 thru 9, 16	D
		Repair				1.5		1	F
010301	CONNECTOR PANEL ASSEMBLY 398-7508-1	Test				1.0		2	H
		Repair				2.5		1,23 thru 26	
010302	CIRCUIT CARD ASSEMBLY, 1MLDA 398-6820-1	Test				1.0		2,5 thru 10,16	J
		Replace				0.1			
		Repair				1.2		1	
010303	CIRCUIT CARD ASSEMBLY, 1MLDB 398-6820-2								L
010304	CIRCUIT CARD ASSEMBLY, 1GA 398-6545-1								L
010305	CIRCUIT CARD ASSEMBLY, 1GB 398-6545-2								L
010306	CIRCUIT CARD ASSEMBLY, 1RRA 398-6549-1								L
010307	CIRCUIT CARD ASSEMBLY, 2XRD 398-6542-4								L
010308	CIRCUIT CARD ASSEMBLY, 2GA 398-6536-1								L
010309	CIRCUIT CARD ASSEMBLY, 2MLDA 398-6821-1								L
010310	CIRCUIT CARD ASSEMBLY, 4SS2 398-6547-21313	Test				0.5		2,5 thru 10	J
		Adjust				0.3		5 thru 9	E
		Replace				0.1			
		Repair				0.3		1	
010311	CIRCUIT CARD ASSEMBLY, 5GA 398-6538-1								L

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SECTION II MAINTENANCE ALLOCATION CHART
FOR

CONSOLE, SYSTEM STATUS CONTROL OJ-50/FYA-10(V)

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT.	(6) REMARKS
			C	O	F	H	D		
02	CONSOLE MESSAGE OJ-347/FYA-10(V), A2, A4								M
03	CONSOLE ASSEMBLY, CABINET, A3 284312-01	Test Repair				5.0 2.0		2 thru 9 1	C,D,H F
0301	PANEL, CONFIGURATION CONTROL, A3A3 520481-01	Test Repair				0.5 1.0		2 1,23,27 thru 31	H
0302	PANEL, INDICATOR CONTROL A3A2 520482-01	Test Repair				0.5 1.0		2 1,23,27 thru 31	H
0303	PANEL, CONFIGURATION CONTROL A3A1 520480-01	Test Repair				0.5 1.0		2 1,23,27 thru 31	H
0304	PANEL CLOCK ASSEMBLY, A3A5 284338-01	Repair				1.0		1	
030401	CLOCK, DIGITAL, ELECTRIC	Replace				0.5		1	
0305	INTERCOMMUNICATION STATION LS-661/FYA A3A6								N
0306	POWER SUPPLY PP-7603/U A3PS1	Test Adjust Replace Repair				0.2 0.5 0.4 1.0		2,3,5,11, 12 2,3,5,11, 12 1 1 thru 5, 10,11,12, 19 thru 22	E
0307	POWER SUPPLY PP-7604/U A3PS2	Test Adjust Replace Repair				0.2 0.5 0.4 1.0		2,3,5,11, 12 2,3,5,11, 12 1 1 thru 5, 10,11,12, 19 thru 22	E
0308	CIRCUIT CARD ASSEMBLY AND INTERFACE A3A4 284308-01	Test Repair Replace				0.5 1.0 1.5		5 thru 9, 13,15 1,18,23, 27 thru 31 1,18	D F
030801	CIRCUIT CARD ASSEMBLY CONTROL SYSTEM A3A4A1 520474-01	Repair				1.0		1,17	
0309	TERMINAL, DIGITAL DATA A3A7, A3A8 AN/FYQ-89								O
0310	BLOWER ASSEMBLY KBB 32-32-2	Replace Repair				0.5 0.8		1 1	
0311	CONTROLLER ASSEMBLY, POWER SUPPLY A3A9 C-7225/FYA-10(V)	Test Repair				1.0 0.5		2,21 1	P Q
04	PROCESSOR ASSEMBLY A5 398-7739-1	Repair				0.4		1	F
0401	CABINET ASSEMBLY 398-7743-1	Service				0.2		32	B,I
040101	BLOWER ASSEMBLY KBB 32-32-2	Replace Repair				0.5 0.8		1 1	

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SECTION II MAINTENANCE ALLOCATION CHART
FOR

CONSOLE, SYSTEM STATUS CONTROL OJ-50/FYA-10(V)

(1) GROUP NUMBER	(2) COMPONENT/ASSEMBLY	(3) MAINTENANCE FUNCTION	(4) MAINTENANCE CATEGORY					(5) TOOLS AND EQPT.	(6) REMARKS
			C	O	F	H	D		
0402	PROCESSOR PANEL NO. 2 398-7438-1	Test Repair				0.5 0.3		1,4,5 1	D,H G
040201	CIRCUIT CARD ASSEMBLY, CON 12C 398-7157-3								K
040202	CIRCUIT CARD ASSEMBLY, CON 12E 398-7157-5								K
040203	CIRCUIT CARD ASSEMBLY, CON 12G 398-7157-7								K
040204	CIRCUIT CARD ASSEMBLY, CON 13A 398-7206-1								K
040205	CIRCUIT CARD ASSEMBLY, CON 6F 398-4350-7	Replace				1.0		1	
0403	FUNCTIONAL ASSEMBLY PROCESSOR 398-7516-1	Test Repair				1.0 1.5		2 thru 9, 16 1	D F
040301	CONNECTOR PANEL ASSEMBLY 398-7519-1	Test Repair				1.0 2.5		2 1,23 thru 26	H
040302	CIRCUIT CARD ASSEMBLY, 1MLDA 398-6820-1								L
040303	CIRCUIT CARD ASSEMBLY, 1MLDB 398-6820-2								L
040304	CIRCUIT CARD ASSEMBLY, 1GA 398-6545-1								L
040305	CIRCUIT CARD ASSEMBLY, 1 GB 398-6545-2								L
040306	CIRCUIT CARD ASSEMBLY, 1RRA 398-6549-1								L
040307	CIRCUIT CARD ASSEMBLY, 2XRD 398-6542-4								L
040308	CIRCUIT CARD ASSEMBLY, 2GA 398-6536-1								L
040309	CIRCUIT CARD ASSEMBLY, 2MLDA 398-6821-1								L
040310	CIRCUIT CARD ASSEMBLY, 4SS2 398-6547-21313								R
040311	CIRCUIT CARD ASSEMBLY, 5GA 398-6538-1								L
05	POWER SUPPLY PP-4751/FYA-10(V) A5PS1								P,S
06	POWER SUPPLY PP-4754/FYA-10(V) A5PS2								P,S
07	POWER SUPPLY PP-4755/FYA-10(V) A5PS3								P,S

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SECTION III TOOL AND TEST EQUIPMENT REQUIREMENTS
FOR

CONSOLE, SYSTEM STATUS CONTROL OJ-50/FYA-10(V)

TOOL OR TEST EQUIPMENT REF CODE	MAINTENANCE CATEGORY	NOMENCLATURE	NATIONAL/NATO STOCK NUMBER	TOOL NUMBER
1	H,D	TOOL KIT, ELECTRONIC EQUIPMENT TK-105/G	5180-00-610-8177	
2	H,D	MULTIMETER, DIGITAL AN/PSM-45	6625-01-139-2512	
3	H,D	VOLTMETER TS-2843/U	6625-00-965-8304	883AB (89536)
4	H,D	MULTIMETER ME-303A/U	6625-00-969-4105	410C (28480)
5	H,D	OSCILLOSCOPE AN/USM-281C	6625-00-106-9622	7603N11S (80009)
6	H,D	OSCILLOSCOPE OS-266(P)/U	6625-01-015-6562	7844 (80009)
7	H,D	DUAL TRACE AMPLIFIER AM-6785/U (2 EA)	6625-00-361-5318	7A26 (80009)
8	H,D	DELAYED TIME BASE	6625-01-081-7818	7B80 OPT02 (80009)
9	H,D	DELAYING TIME BASE	6625-01-032-4342	7B85 (80009)
10	H,D	TEST SET, TRANSISTOR TS-1836D/U	6625-00-138-7320	
11	H,D	LEAD, CLIP, MINICLIP TO BANNANA	6625-01-014-2669	3782-60 RED (05276)
12	H,D	LEAD, CLIP, MINICLIP TO BANNANA	6625-01-030-7081	3782-60 BLK (05276)
13	H,D	CLIP, IC TEST (14/16 PIN)	5999-00-286-4302	3916A (05276)
14	H,D	PROBE, 1X, PASSIVE	6625-00-163-1448	010-6101-01(80009)
15	H,D	PROBE, LOGIC TTL/DTL	6625-00-433-4282	10525T (28480)
16	H,D	EXTENDER, CARD	6625-00-954-7121	398-5589-1 (11530)
17	H,D	EXTRACTOR/INSERTER, DIP	5120-00-110-8369	706-3739-01-00-0 (71279)
18	H,D	EXTRACTOR, FLAT CABLE	6930-00-511-6065	3438 (75037)
19	H,D	AMMETER, DIRECT CURRENT MD-511/U	6625-00-781-5769	931-2912001 (65092)
20	H,D	RESISTOR, VARIABLE, 0-1 OHM, 750 WATT	*	MOD T1 1300 (44655)
21	H,D	TRANSFORMER, VARIABLE, POWER TF-510/U	6120-00-054-7794	W10MT3A (24655)
22	H,D	POWER SUPPLY	6130-00-496-0549	5005R (98095)
23	H,D	TOOL WIRE WRAP, PORTABLE ELECTRIC	5130-00-116-7474	14XA-2B (24047)
24	H,D	TOOL, WIRE UNWRAP, MANUAL	5130-00-118-7075	505084-(LH) (24047)
25	H,D	SLEEVE, WIRE WRAPPING	5130-00-731-5941	500350 (24047)
26	H,D	BIT, WIRE WRAPPING	5130-00-731-5942	519936 (24047)
27	H,D	TOOL, WIRE UNWRAP, MANUAL	5120-00-104-9022	500130 (24047)
28	H,D	SLEEVE, WIRE WRAPPING	5130-00-987-7059	18640 (24047)
29	H,D	BIT, WIRE WRAPPING	5130-00-018-5852	26699 (24047)
30	H,D	SLEEVE, WIRE WRAPPING	5130-00-987-7057	18840 (24047)
31	H,D	BIT, WIRE WRAPPING	5120-00-051-3858	26263 (24047)
32	H	CLEANER, VACUUM, HAND	7910-00-205-3400	

* THE NATIONAL STOCK NUMBERS THAT ARE MISSING FROM THIS LIST HAVE BEEN REQUESTED AND WILL BE ADDED BY A CHANGE TO THIS LIST UPON RECEIPT.

NOTE

EQUIVALENT TOOLS OR TEST EQUIPMENT MAY BE SUBSTITUTED FOR THE ABOVE.

DA FORM 6013 1 Oct 77

(Edition of 1 Oct 74 may be used until exhausted)

MISA-Pm 2133-77

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SECTION IV. REMARKS

REFERENCE CODE	REMARKS
A	INSPECT FOR ABNORMAL CONDITIONS.
B	CLEAN AS REQUIRED.
C	OPERATIONAL TESTS; POWER SUPPLIES.
D	FAULT ISOLATE TO DEFECTIVE LRU.
E	ADJUST TO SPECIFIED TOLERANCES.
F	REPAIR BY REPLACING DEFECTIVE LRU.
G	REPAIR BY REPLACING LAMPS, FUSES, AND SWITCHES.
H	TEST FOR CONTINUITY.
I	LUBRICATE AS REQUIRED.
J	REFER TO TM 11-5895-402-15/1, -15/2, AND TM 11-5895-554-15/1, -15/2, -15/3.
K	MAINTENANCE FUNCTIONS, CATEGORY, AND T&TE REQUIREMENTS ARE SAME AS FOR GROUP NUMBER 010201.
L	MAINTENANCE FUNCTIONS, CATEGORY, AND T&TE REQUIREMENTS ARE SAME AS FOR GROUP NUMBER 010302.
M	SEE TM 11-5895-839-14 FOR TEST REQUIREMENTS AND PROCEDURES, AND TM 11-5895-839-40P FOR REPAIR PARTS.
N	SEE TM 11-5895-416-14 FOR TEST REQUIREMENTS AND PROCEDURES, AND TM 11-5895-416-40P FOR REPAIR PARTS.
O	SEE TM 11-5895-10941-14 FOR TEST REQUIREMENTS AND PROCEDURES, AND TM 11-5895-1094-40P FOR REPAIR PARTS.
P	REFER TO TM 11-5895-552-15/1, -15/2, -15/3 FOR TEST REQUIREMENTS AND PROCEDURES.
Q	REMOVE, REPAIR AND REPLACE.
R	MAINTENANCE FUNCTIONS, CATEGORY, AND T&TE REQUIREMENTS ARE SAME AS FOR GROUP NUMBER 010310.
S	REFER TO TM 11-5895-552-40P FOR REPAIR PARTS.

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RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

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DATE SENT
10 July 1975

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-5840-340-12	23 Jan 74	Radar Set AN/PRC-76

BE EXACT PIN-POINT WHERE IT IS

PAGE NO	PARA-GRAPH	FIGURE NO	TABLE NO	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2^{o} IFF antenna lag rather than 1^{o}. REASON: Experience has shown that with only a 1^{o} lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting is minimized by adjusting the lag to 2^{o} without degradation of operation.
3-10	3-3		3-1	Item 5, Function column. Change "2 db" to "3db." REASON: The adjustment procedure for the TRANS POWER FAULT indicator calls for a 3 db (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

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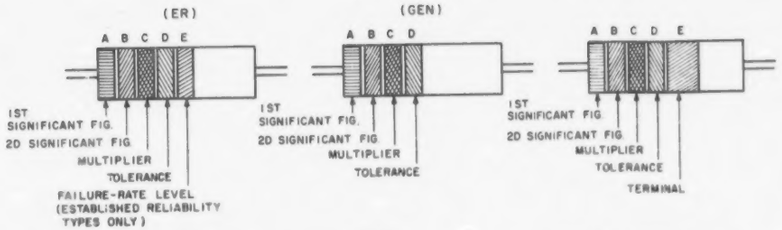


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

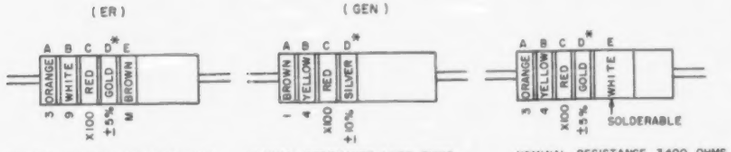
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING

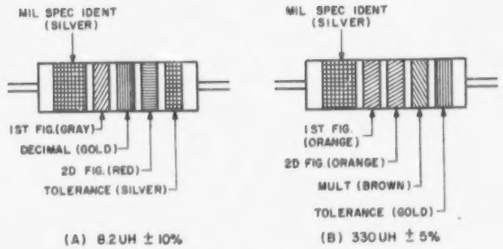


COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

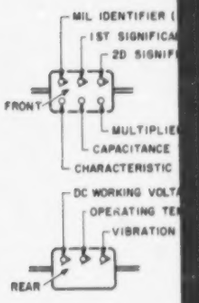
COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIX

EM



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CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

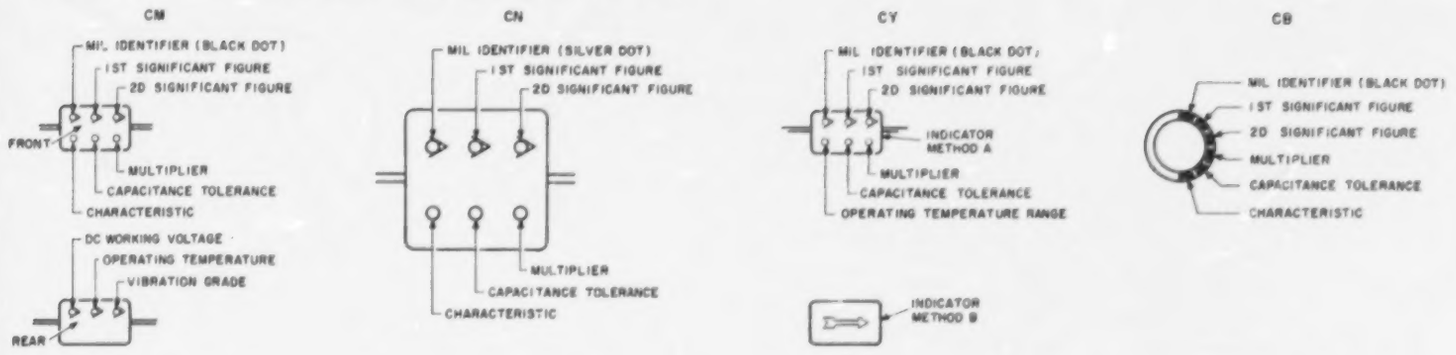

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY CB	0	0	1			±20%	±20%		A			$-55°_{TO}+70°C$	10-55 Hz
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				$-55°_{TO}+85°C$	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				$-55°_{TO}+125°C$	10-2,000Hz
GREEN		5	5		±5%				F			500		
BLUE		6	6										$-55°_{TO}+150°C$	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						

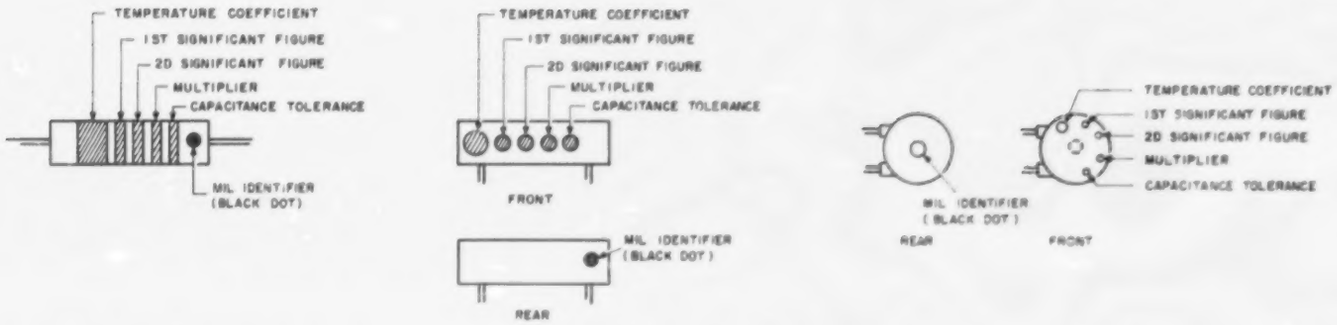

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-290, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

ESC-FM 913-73

Figure FO-1. Color Code Markings for MIL-STD Resistors, Inductors, and Capacitors.

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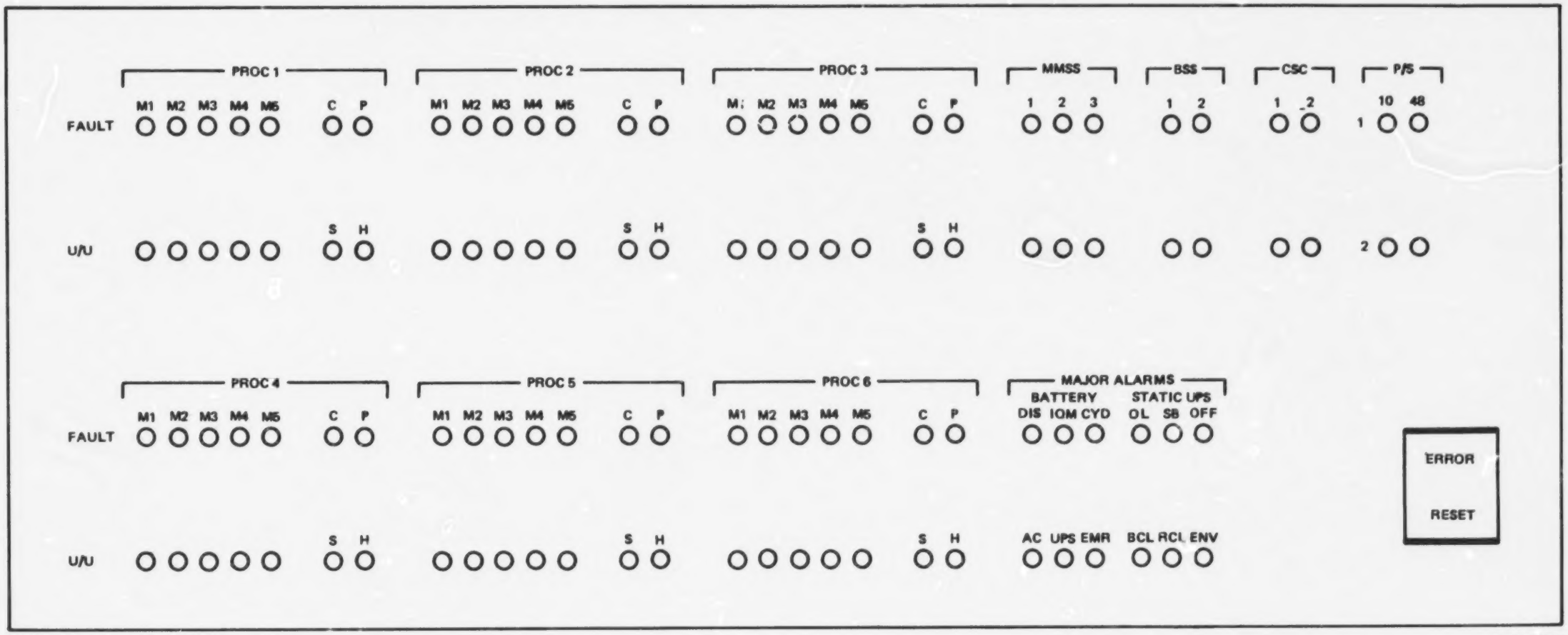

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Figure FO-2. Fault Indicator Panel, Controls and Indicators.

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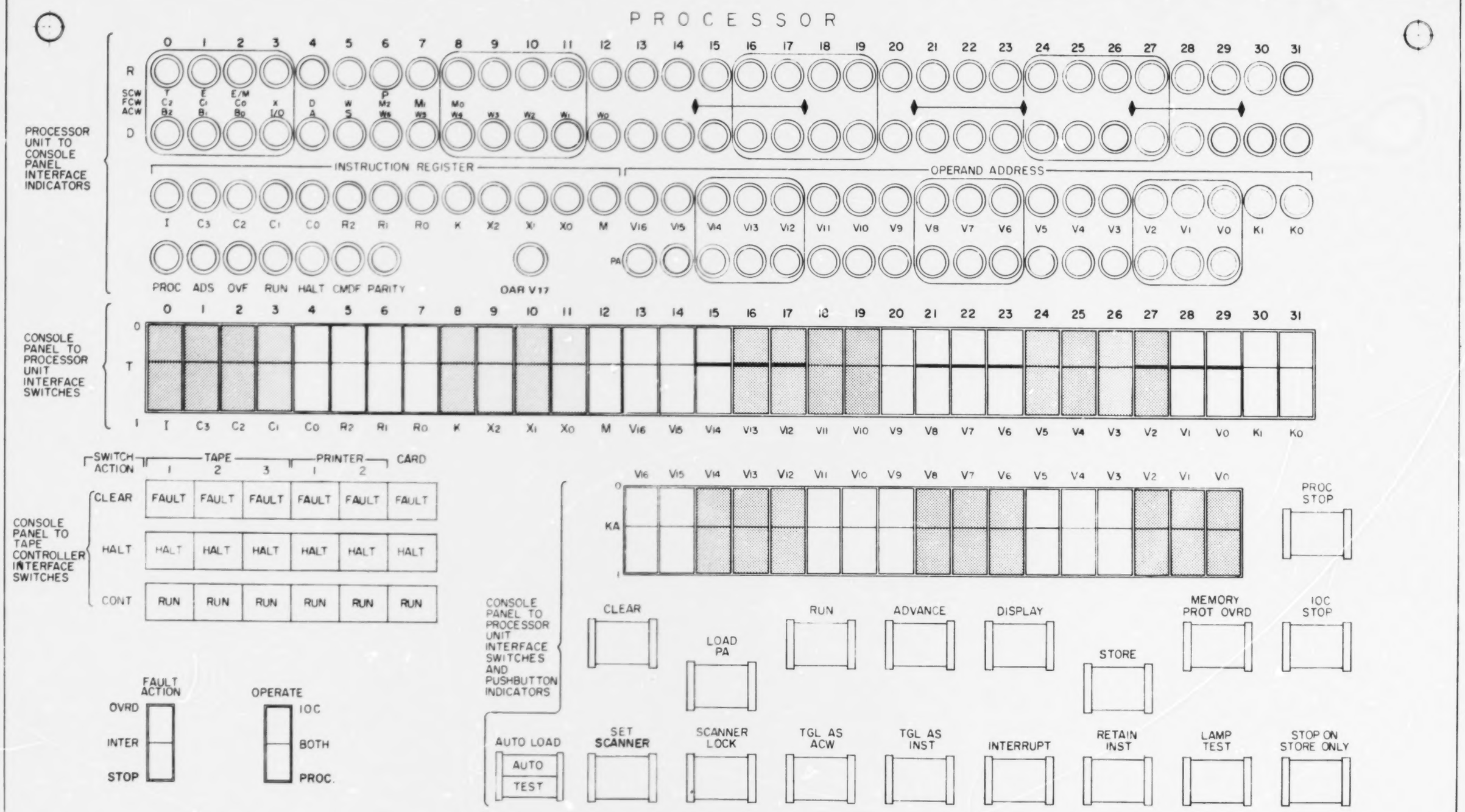

EL5VL010

Figure FO-3. Processor Panel, Controls and Indicators.

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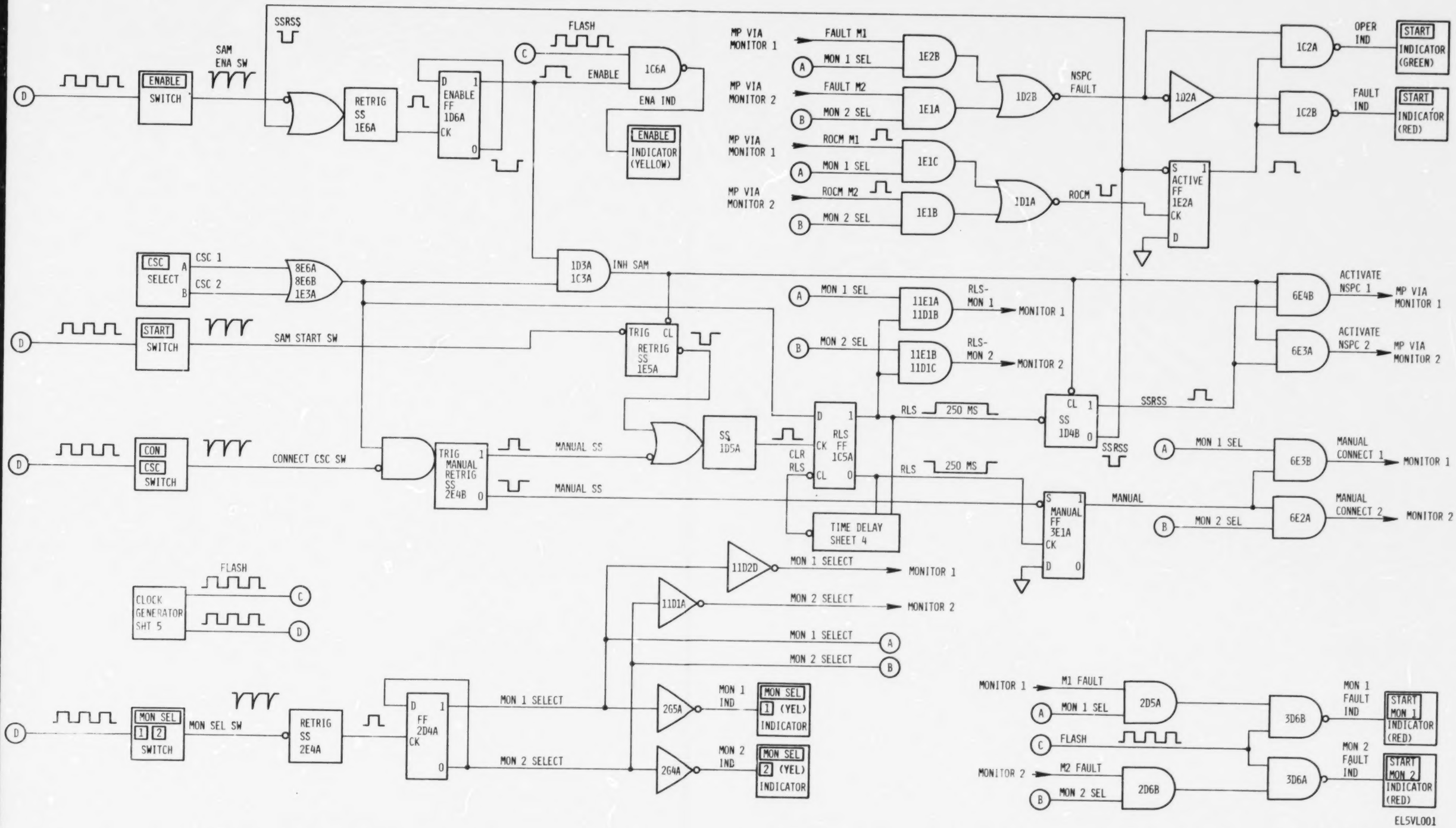

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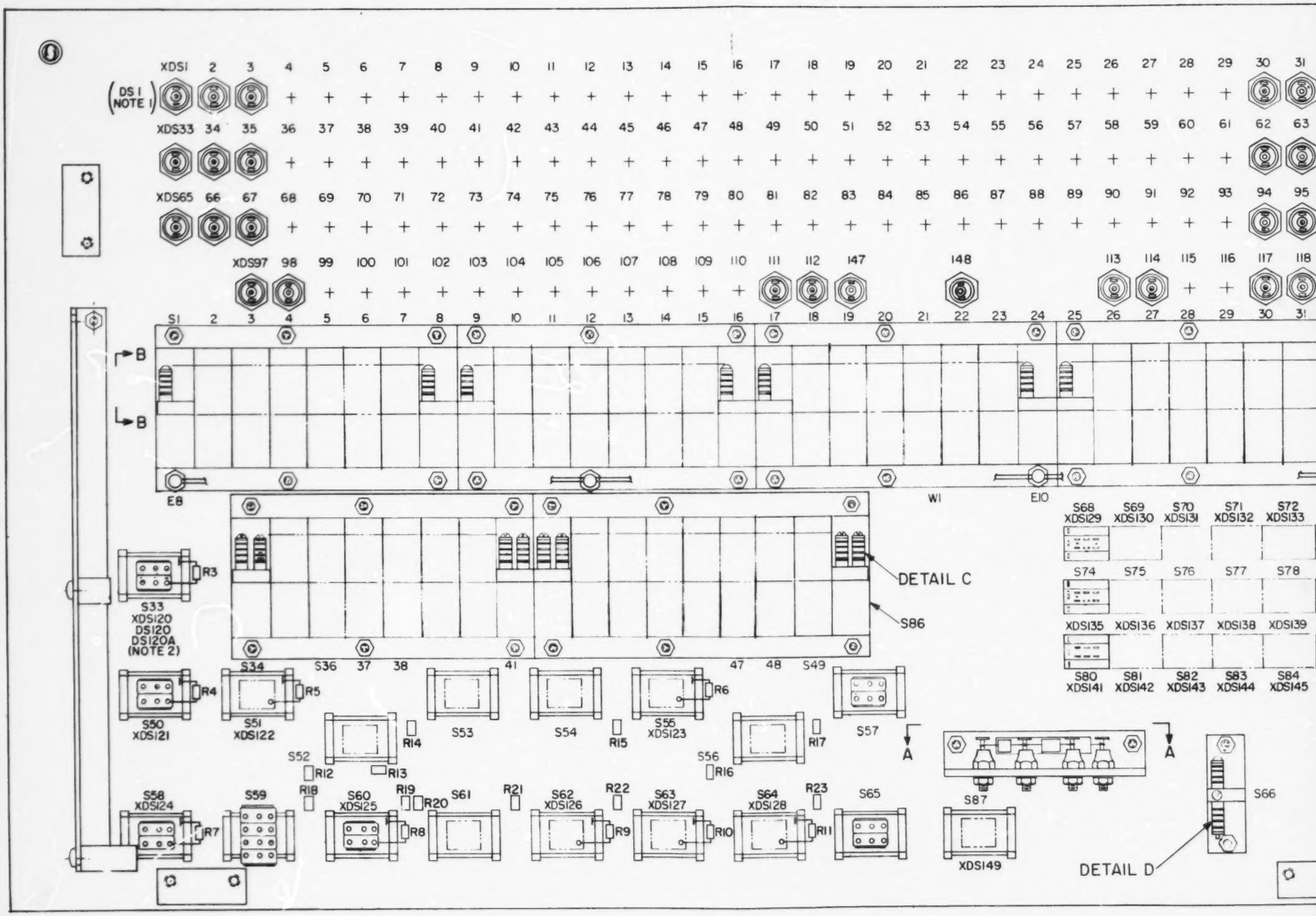
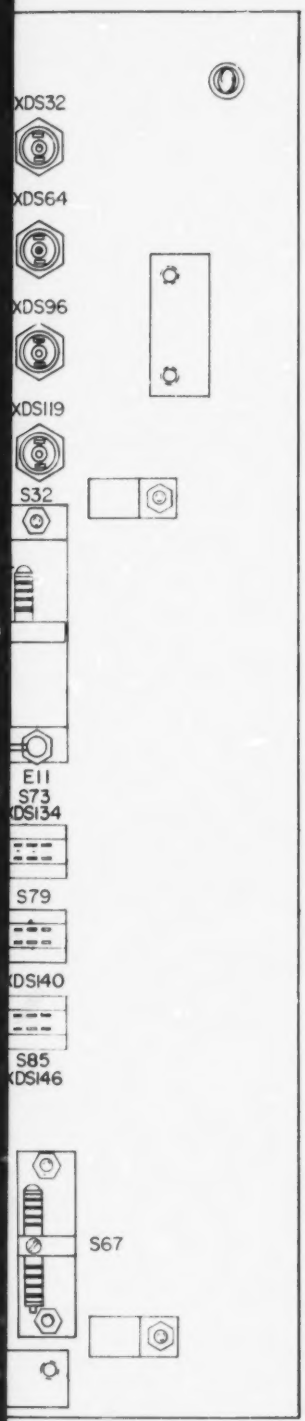
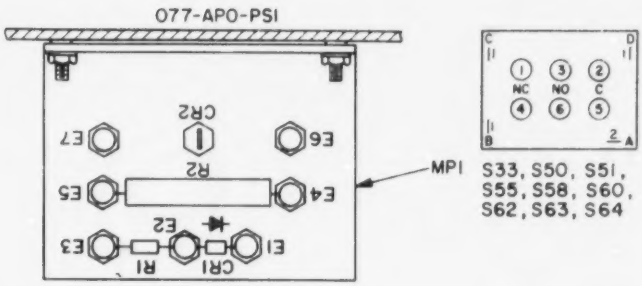
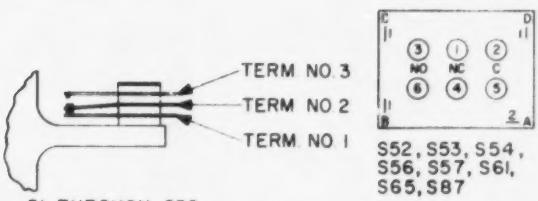
Figure FO-4. SSCC Logic, Block Diagram.


XDS1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
(DS1 NOTE 1)
XDS33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
XDS65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
XDS97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 147 148 113 114 115 116 117 118
S1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
B
B
E8
W1
E10
S68 XDS129
S69 XDS130
S70 XDS131
S71 XDS132
S72 XDS133
S74
S75
S76
S77
S78
XDS135
XDS136
XDS137
XDS138
XDS139
S80 XDS141
S81 XDS142
S82 XDS143
S83 XDS144
S84 XDS145
DETAIL C
S86
R3
S33 XDS120 DS120 DS120A (NOTE 2)
S34
S36 37 38 41 47 48 S49
R4
S50 XDS121
R5
S51 XDS122
S52
R12
R13
R14
S53
S54
R15
R6
S55 XDS123
S56
R16
R17
S57
A
A
S87
XDS149
S66
DETAIL D
R18
R19
R20
S61
R21
R22
R23
S58 XDS124
R7
S59
S60 XDS125
R8
S62 XDS126
R9
S63 XDS127
R10
S64 XDS128
R11
S65

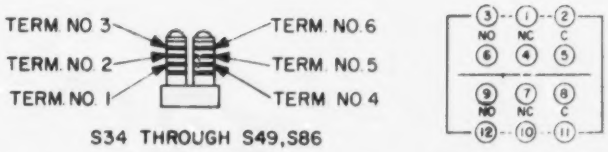




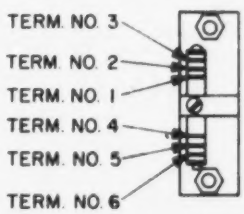
SECTION A-A



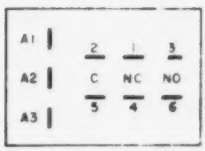
S1 THROUGH S32
VIEW B-B



S34 THROUGH S49, S86
DETAIL C



S66 AND S67
DETAIL D



S68 THROUGH S85

NOTES:
1. DS1 TYPICAL FOR DS1 THROUGH DS119 AND DS147.
2. DS120 AND DS120A TYPICAL FOR DS120 THROUGH DS146.

EL5VL053

Figure FO-5. Processor Panel, Parts Location, Rear View.

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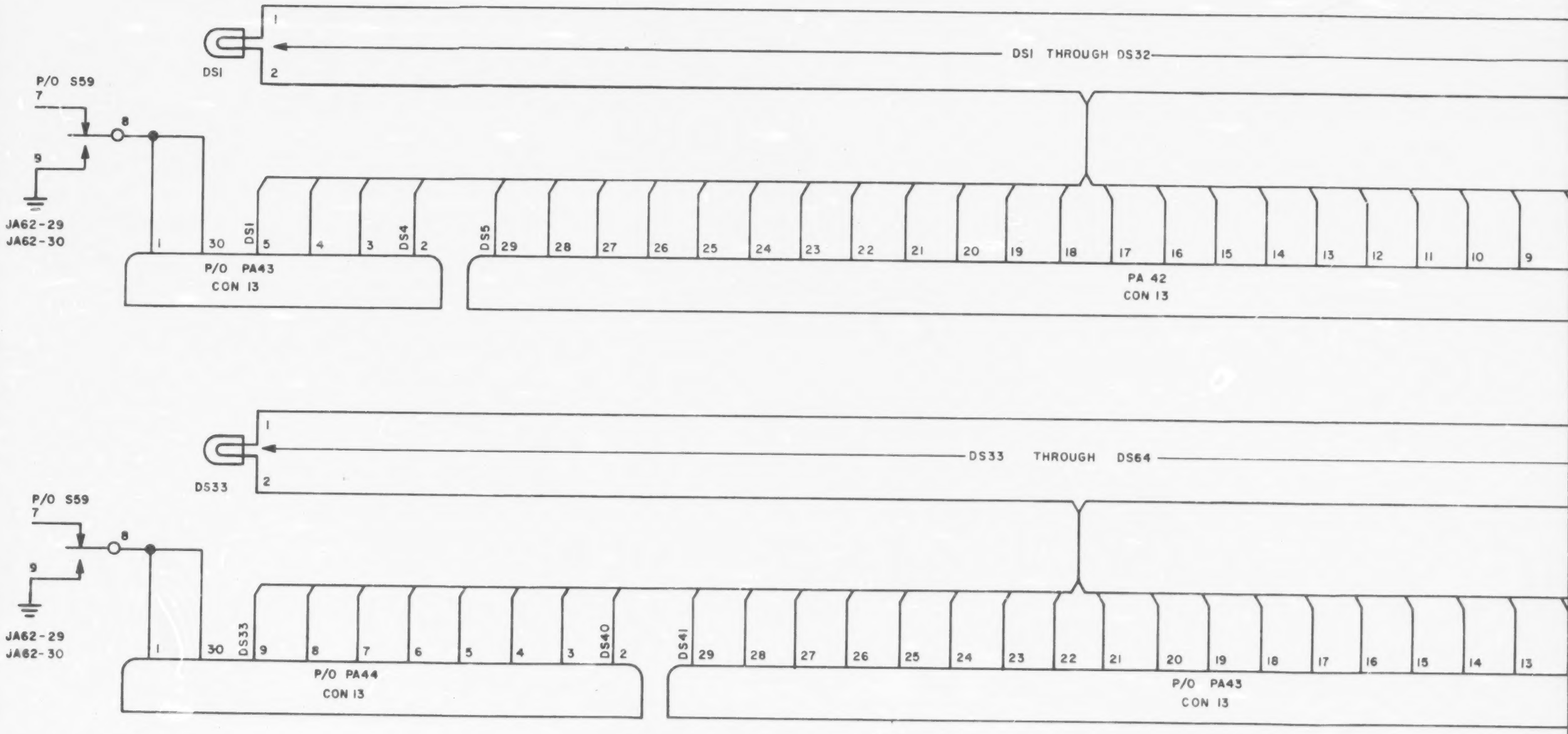
DSI
1
2
DSI THROUGH DS32
P/O S59
7
8
9
JA62-29
JA62-30
1
30
DSI
5
4
3
DS4
2
P/O PA43
CON 13
DS5
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
PA 42
CON 13
DS33
1
2
DS33 THROUGH DS64
P/O S59
7
8
9
JA62-29
JA62-30
1
30
DS33
9
8
7
6
5
4
3
DS40
2
P/O PA44
CON 13
DS41
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
P/O PA43
CON 13

Figure

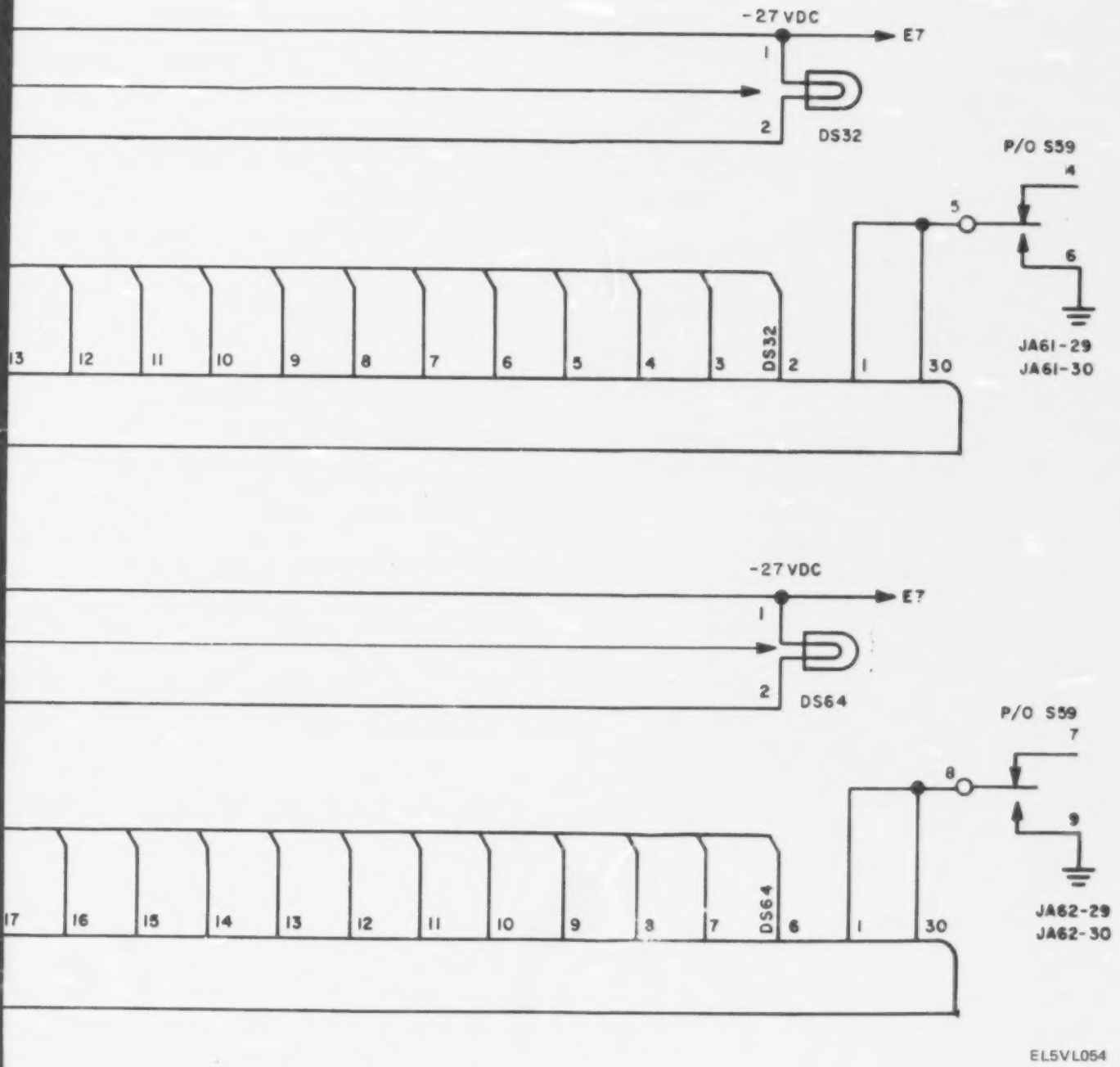

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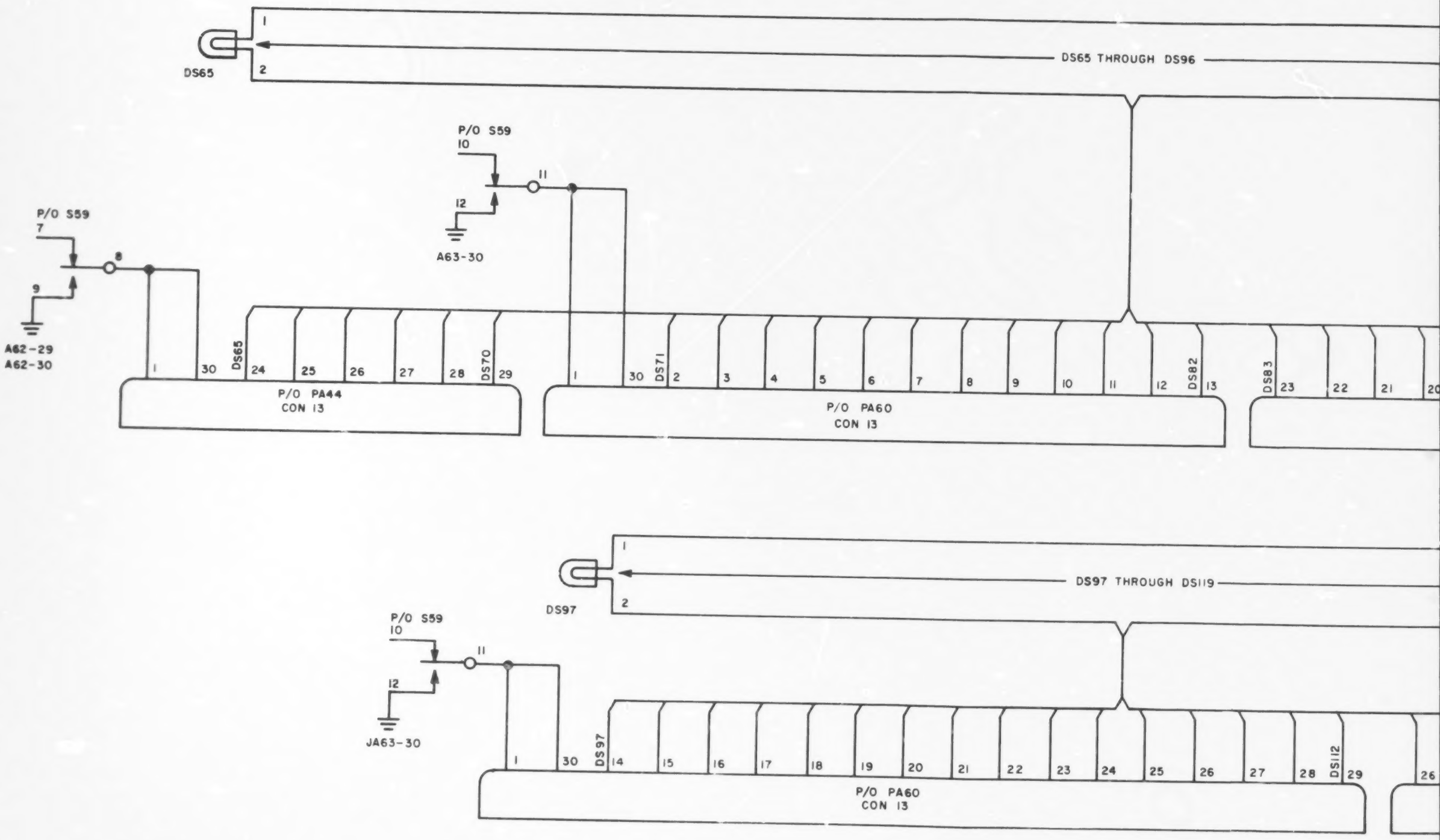
Figure FO-6(1). Processor Panel, Schematic Diagram (Sheet 1 of 7).


DS65
1
2
DS65 THROUGH DS96
P/O S59
10
11
12
A63-30
P/O S59
7
8
9
A62-29
A62-30
1
30
DS65
24
25
26
27
28
DS70
29
P/O PA44
CON 13
1
30
DS71
2
3
4
5
6
7
8
9
10
11
12
DS82
13
DS83
23
22
21
20
P/O PA60
CON 13
DS97
1
2
DS97 THROUGH DS119
P/O S59
10
11
12
JA63-30
1
30
DS97
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
DS112
29
26
P/O PA60
CON 13

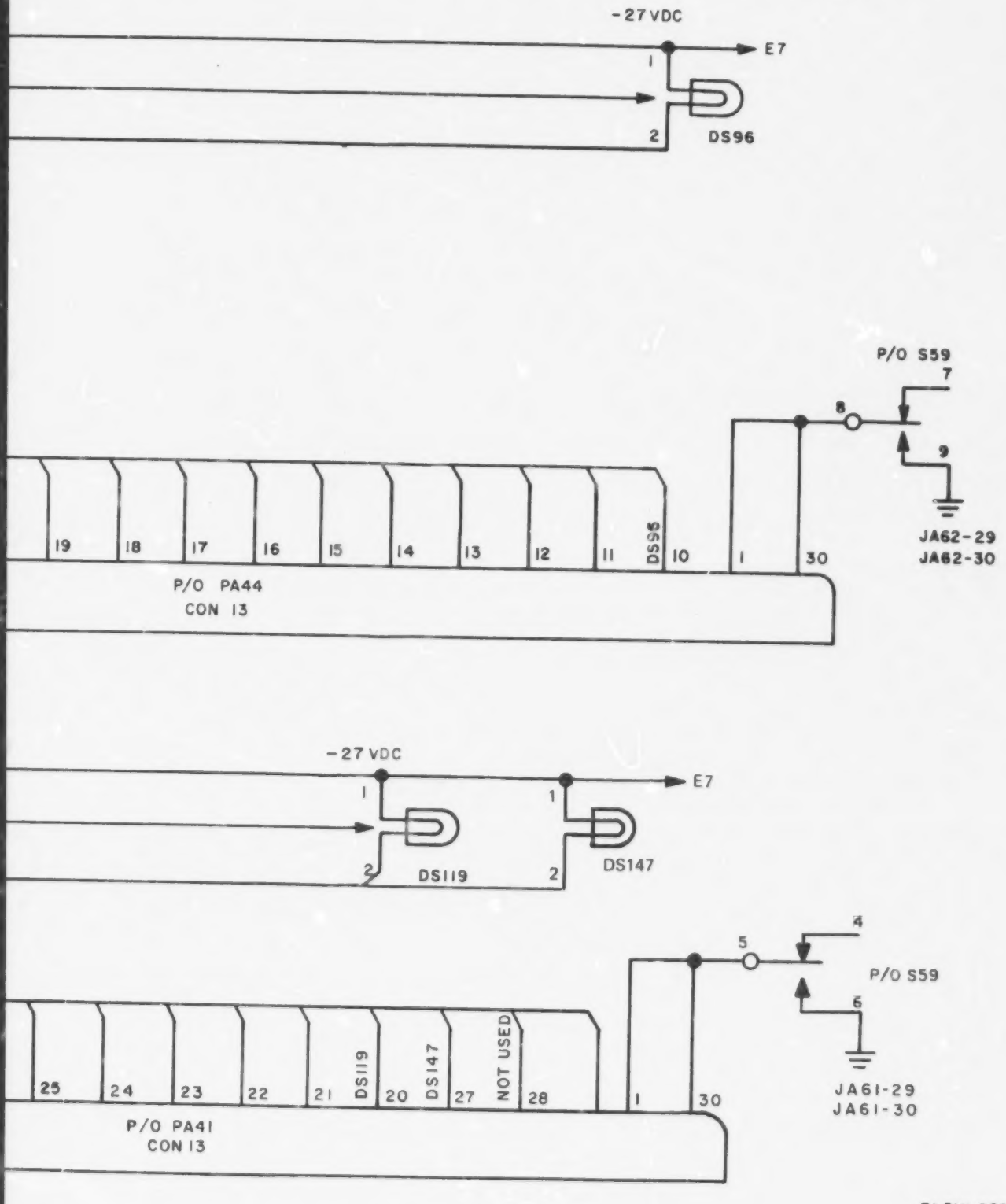


Figure FO-6(2). Processor Panel, Schematic Diagram (Sheet 2 of 7).

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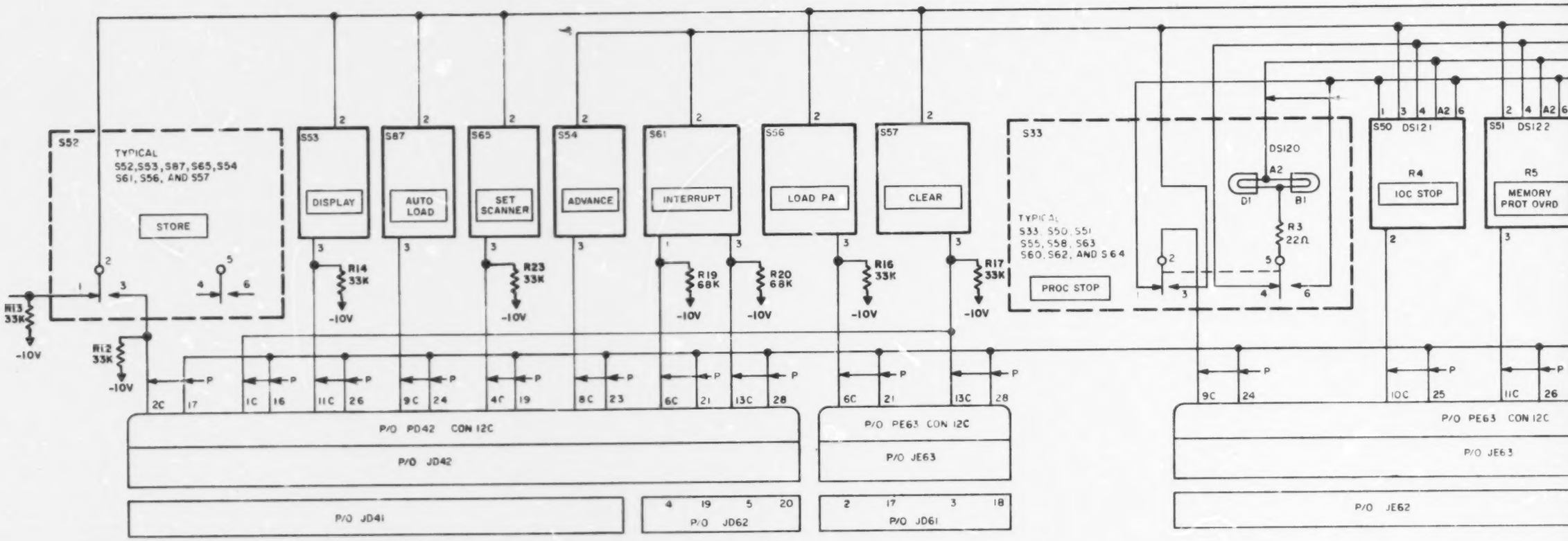
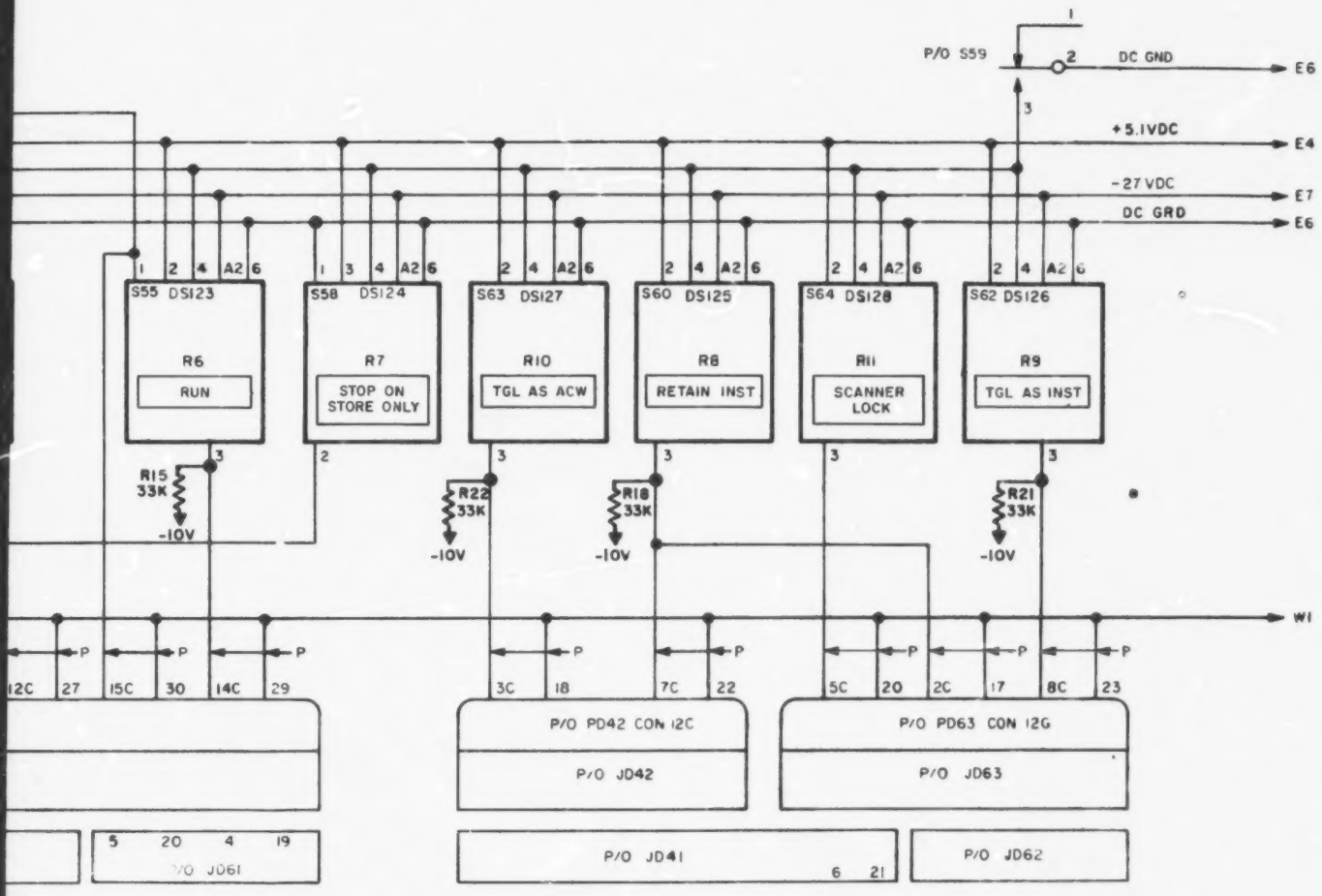


NOTES:

1. PIN NUMBERS BETWEEN PLUGS AND JACKS COINCIDE UNLESS OTHERWISE NOTED.
2. INPUT PINS FOLLOWED BY A LETTER HAVE THEIR OUTPUTS APPEARING ON THE SAME PIN NUMBER LESS THE LETTER.



EL5VL056

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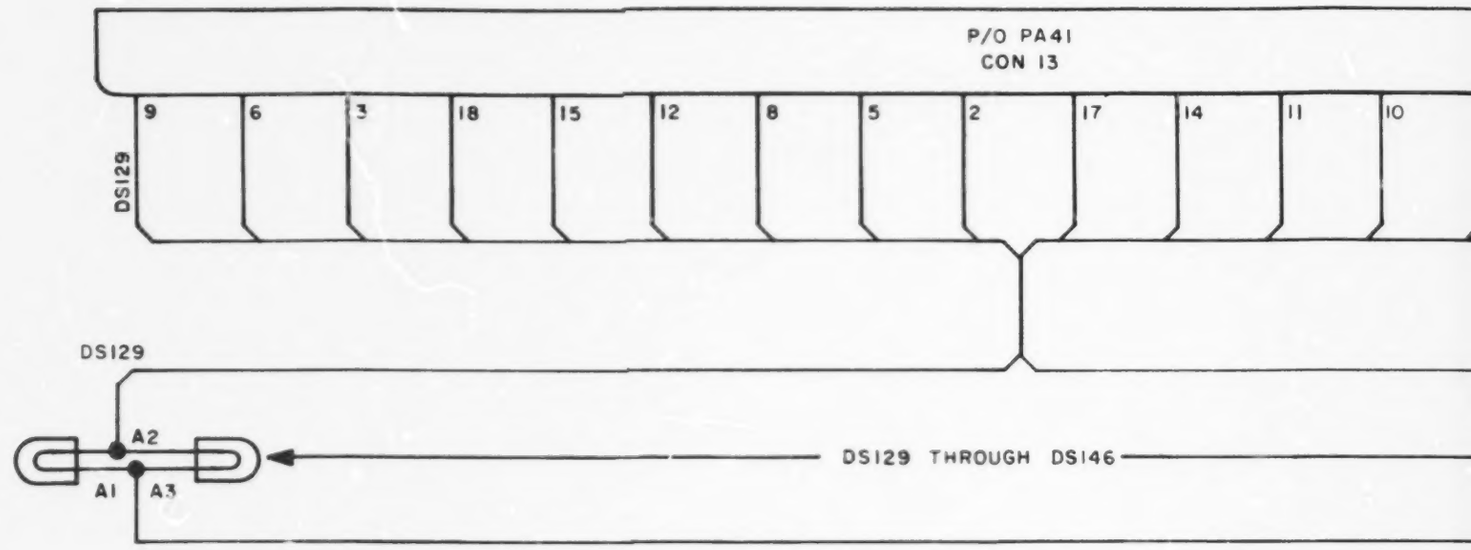
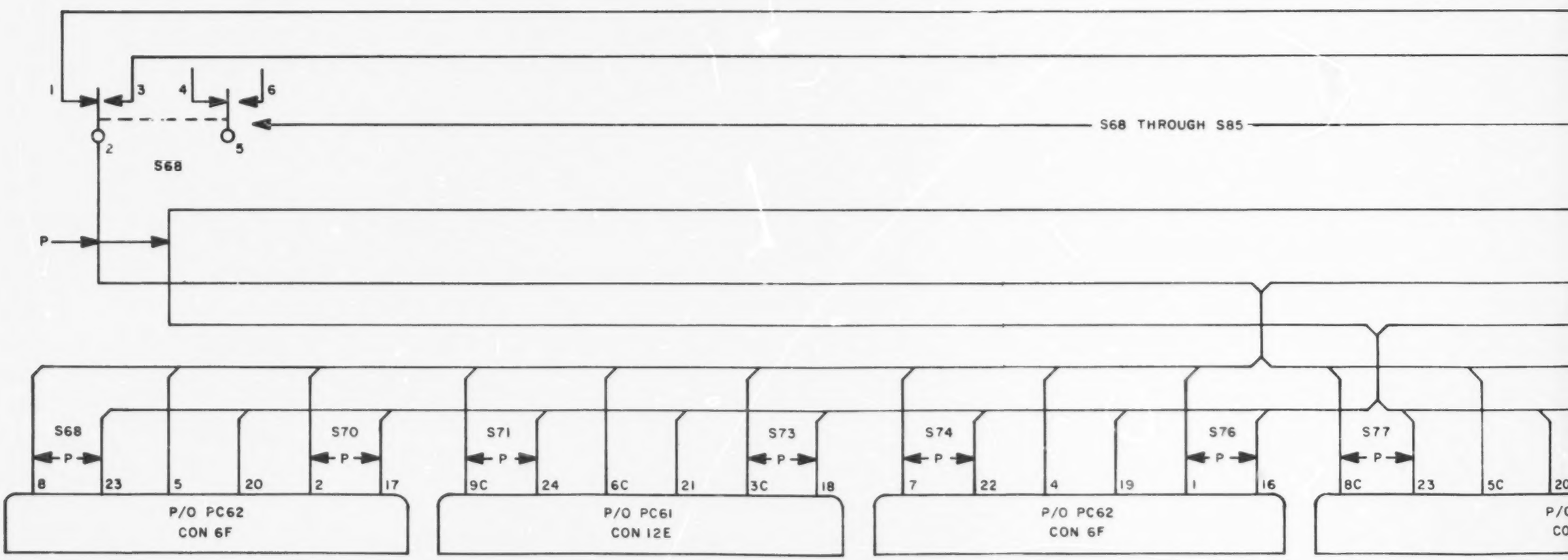
Figure FO-6(3). Processor Panel, Schematic Diagram (Sheet 3 of 7).

NOTE:
INPUT PINS FOLLOWED BY A LETTER HAVE THEIR OUTPUTS APPEARING ON THE SAME PIN NUMBER LESS THE LETTER.



S79-



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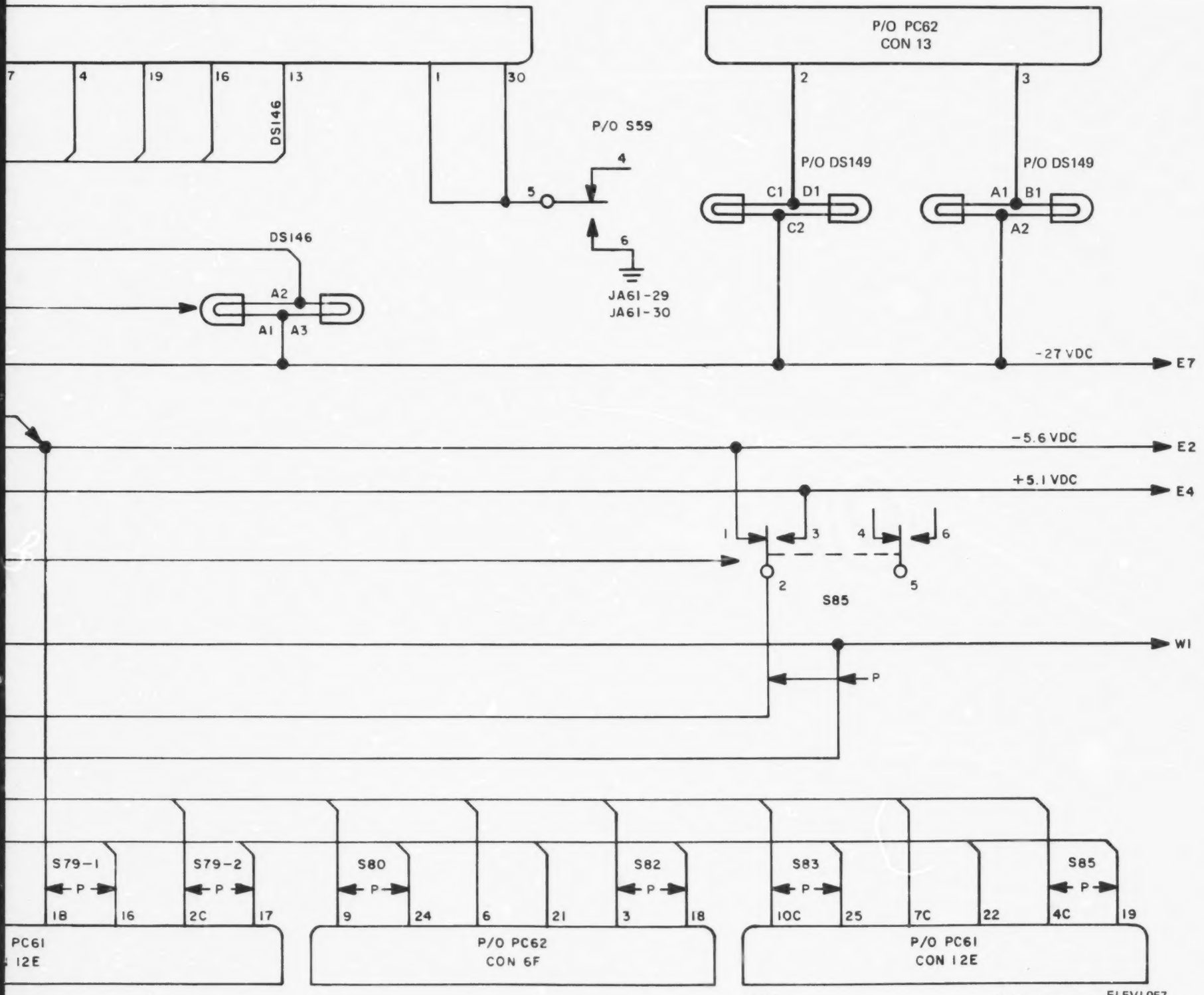

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Figure FO-6(4). Processor Panel, Schematic Diagram (Sheet 4 of 7).

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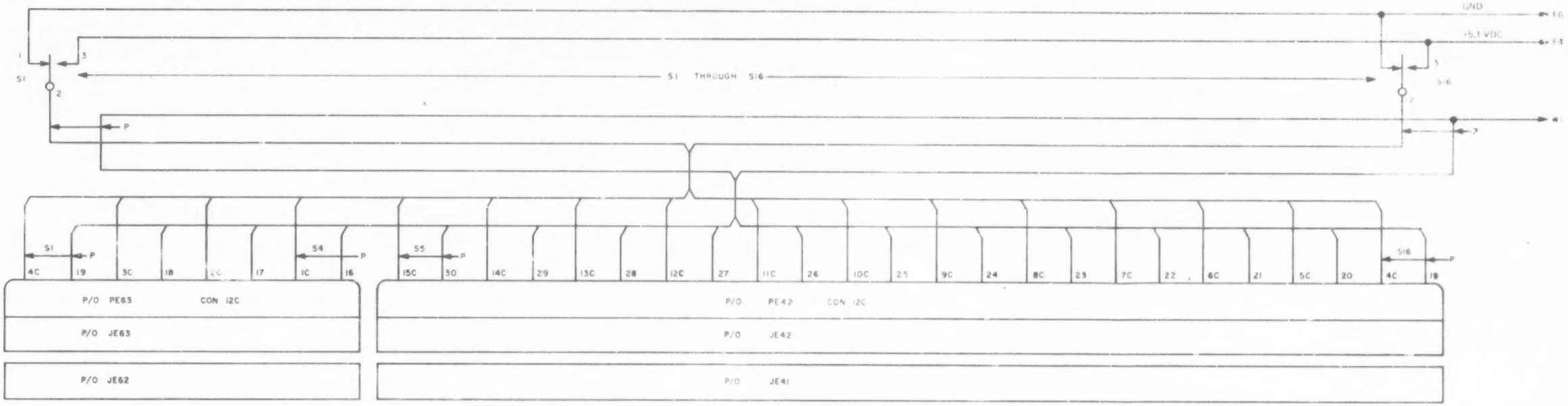
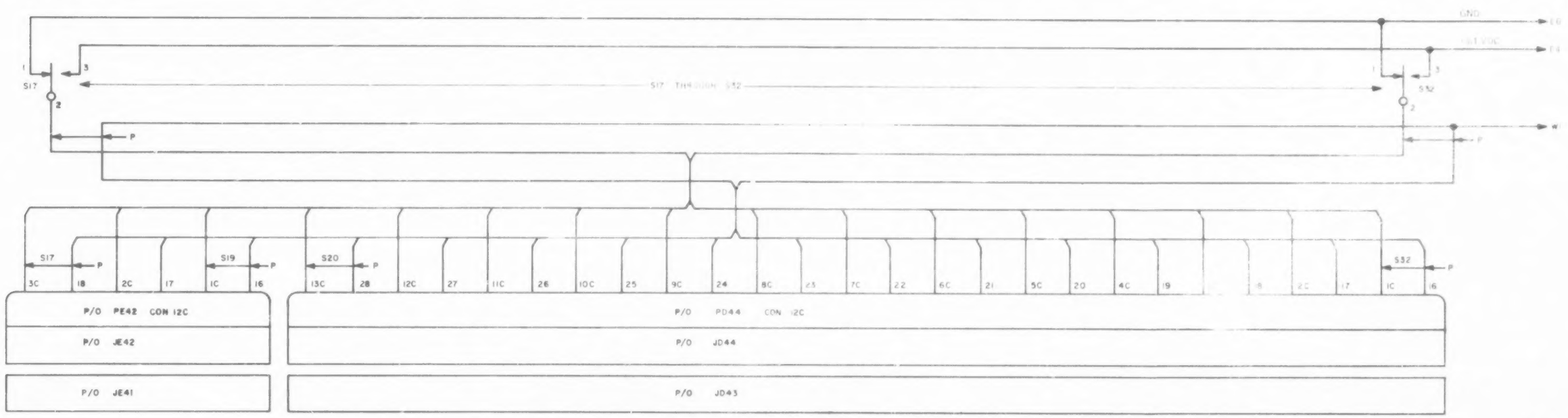
NOTES:
1. PIN NUMBERS BETWEEN PLUGS AND JACKS COINCIDE UNLESS OTHERWISE NOTED.
2. INPUT PINS FOLLOWED BY A LETTER HAVE THEIR OUTPUTS APPEARING ON THE SAME PIN NUMBER LESS LETTER.





EL5VL058

Figure FO-6(5). Processor Panel, Schematic Diagram (Sheet 5 of 7).

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NOTES:
1. PIN NUMBERS BETWEEN PLUGS AND JACKS COINCIDE UNLESS OTHERWISE NOTED.
2. INPUT PINS FOLLOWED BY A LETTER HAVE THEIR OUTPUTS APPEARING ON THE SAME PIN NUMBER, LESS THE LETTER.

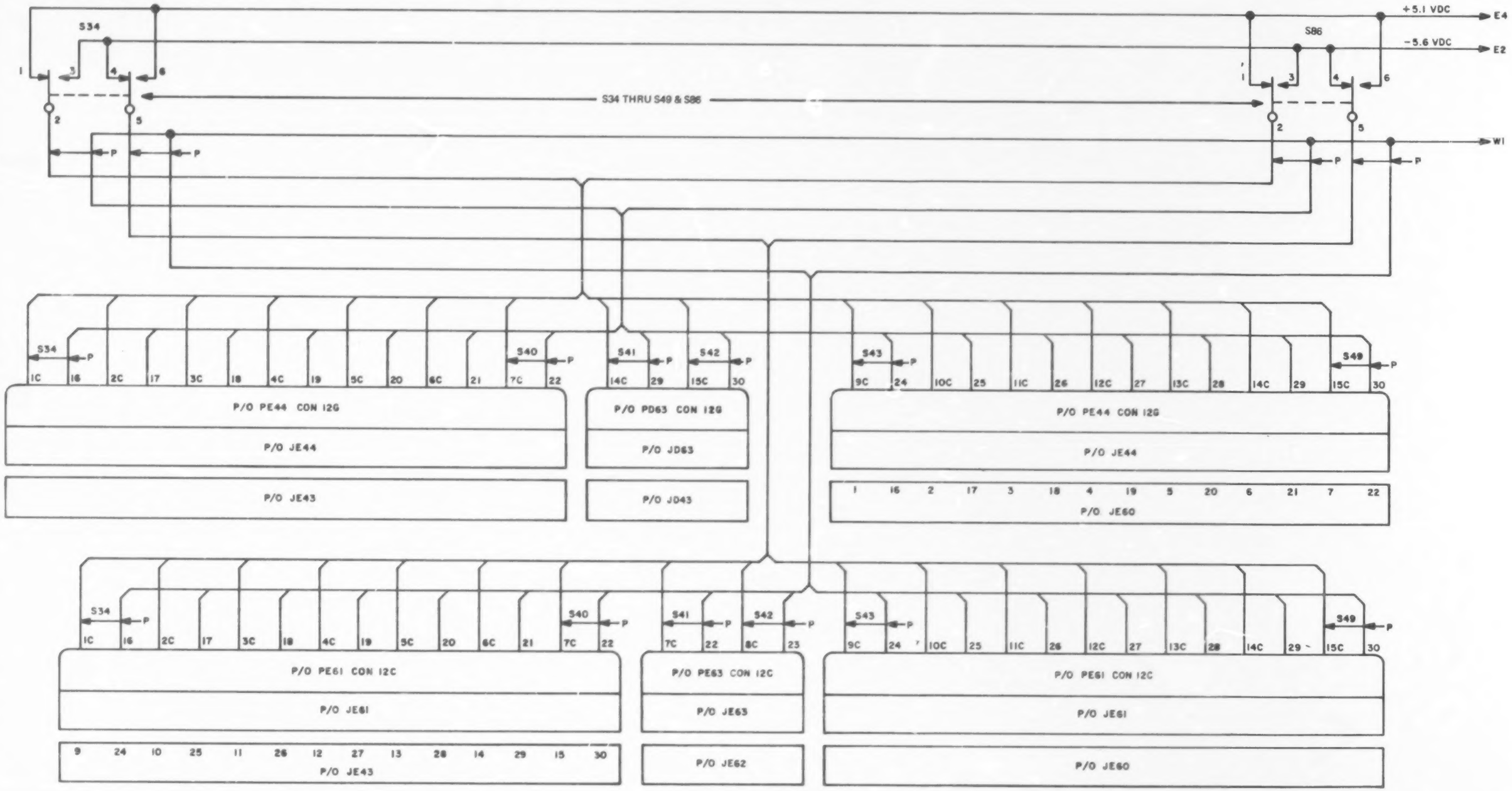

Figure FO-6(6). Processor Panel, Schematic Diagram (Sheet 6 of 7).

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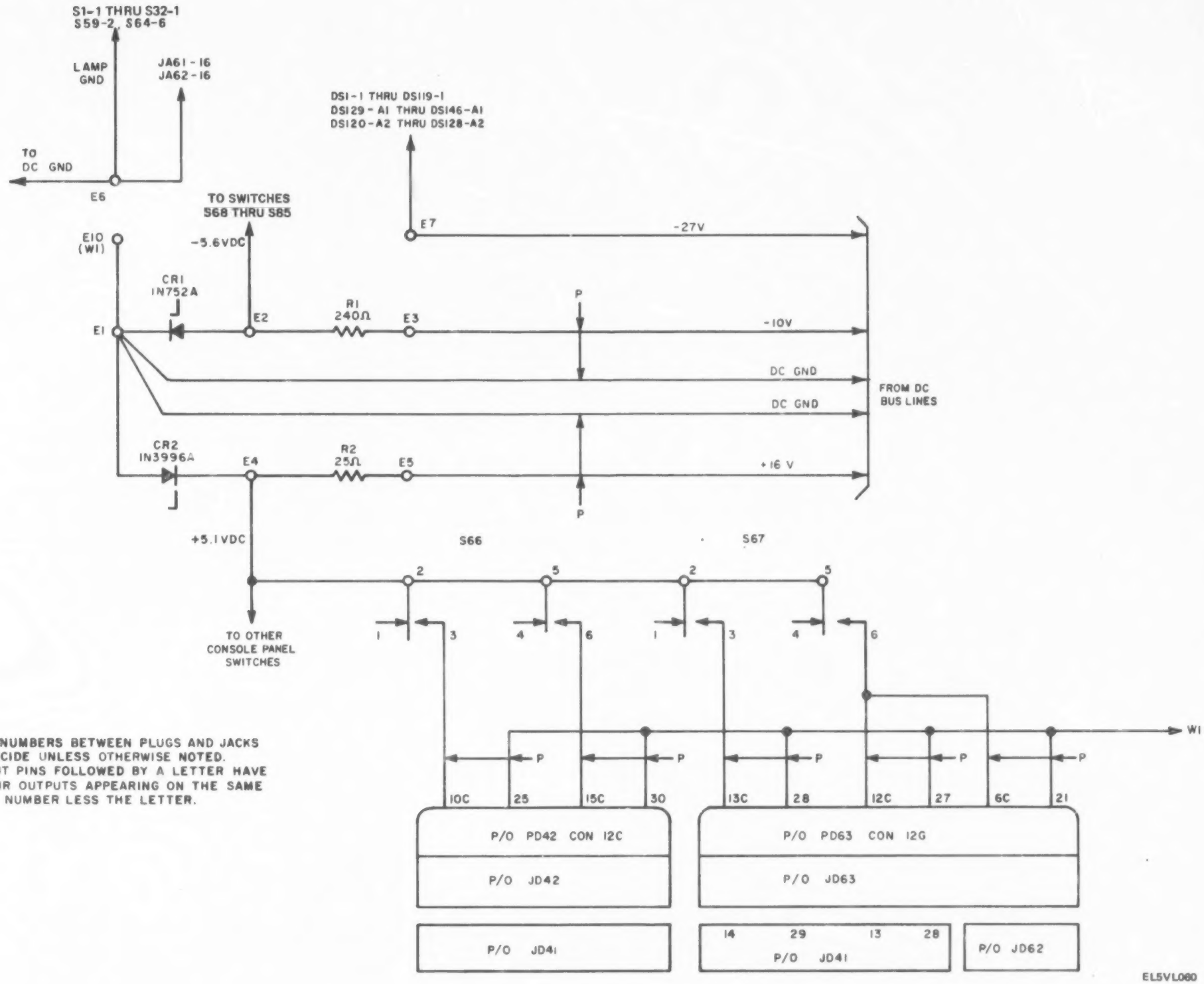

NOTES:
1. PIN NUMBERS BETWEEN PLUGS AND JACKS COINCIDE UNLESS OTHERWISE NOTED.
2. INPUT PINS FOLLOWED BY A LETTER HAVE THEIR OUTPUTS APPEARING ON THE SAME PIN NUMBER LESS THE LETTER.

Figure FO-6(7). Processor Panel, Schematic Diagram (Sheet 7 of 7).

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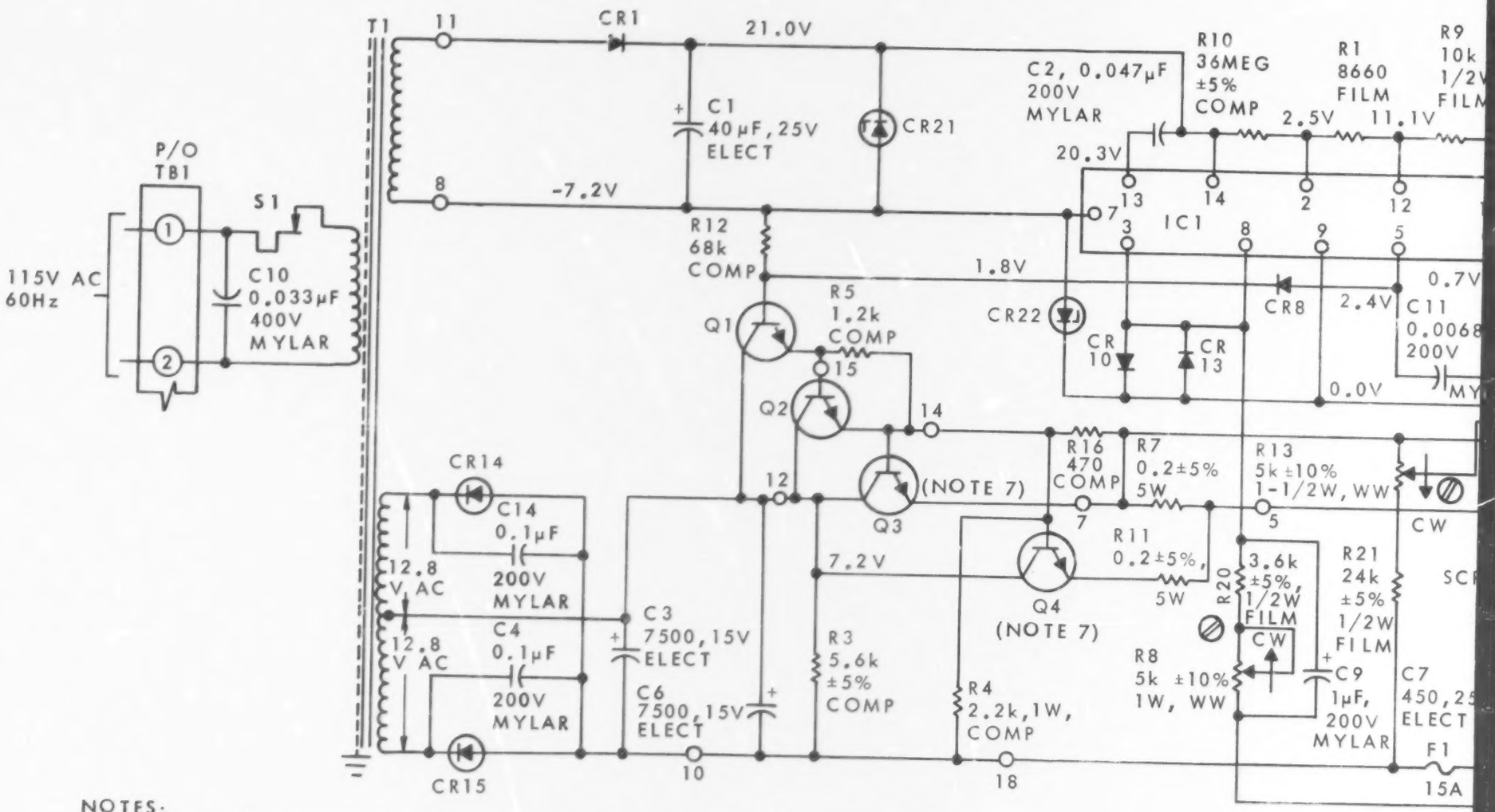
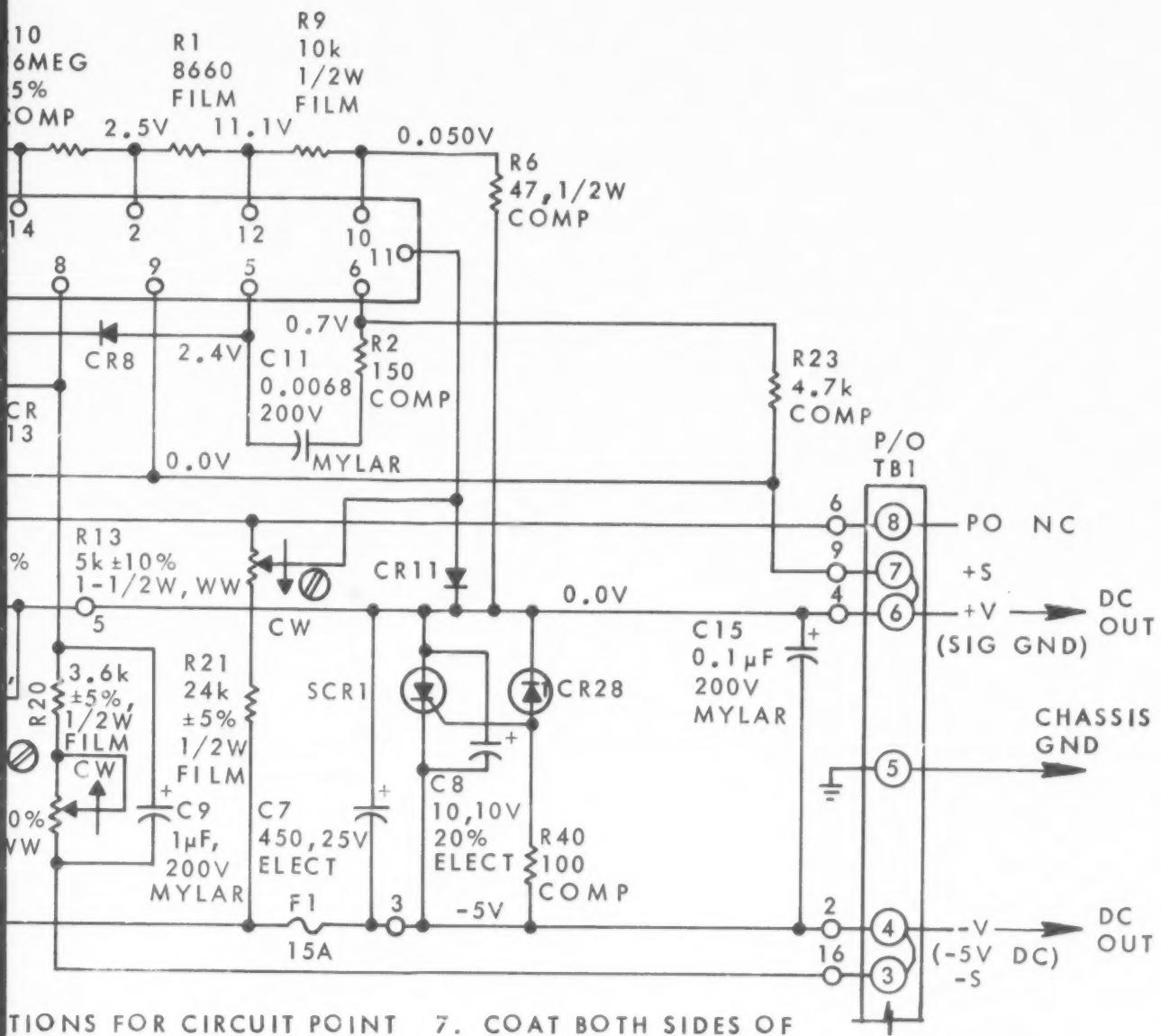


NOTES:

1. RESISTOR VALUES ARE IN OHMS.
2. RESISTOR WATTAGE 1/4 WATT: RESISTORS ABOVE 2 WATTS ARE WIREWOUND UNLESS OTHERWISE NOTED.
3. RESISTOR TOLERANCES: COMP. ±10%; WIREWOUND ±2%; FILM ±1%; UNLESS OTHERWISE NOTED.
4. CAPACITOR TOLERANCES: ELECTROLYTIC -10%,+100%: MYLAR ±10%; CERAMIC 10%; UNLESS OTHERWISE NOTED.
5. SYMBOLS:
   - ⏚ INDICATES CONNECTION TO CHASSIS.
   - ⊘ INDICATES ADJUSTMENT OF CALIBRATION CONTROL.
   - —○— INDICATES TERMINAL ON PRINTED WIRING BOARD.
6. CONDITIONS FOR CIRCUIT PO MEASUREMENTS: INPUT: 115V 60Hz; NOM. RATED VOLTAGE LOAD. INDICATED VOLTAGES TYPICAL VALUES AND ARE DC UNLESS OTHERWISE NOTED DC MEASUREMENTS TAKEN WI 20,000 OHMS/V VOLTMETER BETWEEN +S(TERM 7) AND IND POINTS UNLESS NOTED; +S AN SHORTED, -S AND -V SHORTE VOLTAGES IN PARENTHESES A ONLY TO MODEL LCS-B-6. A SINGLE READING APPLIES TO MODELS.

Figure FO



TIONS FOR CIRCUIT POINT
REMENTS: INPUT: 115V AC,
NOM. RATED VOLTAGE NO
INDICATED VOLTAGES ARE
L VALUES AND ARE
LESS OTHERWISE NOTED.
ASUREMENTS TAKEN WITH
OHMS/V VOLTMETER
N +S(TERM 7) AND INDICATED
UNLESS NOTED; +S AND +V
D, -S AND -V SHORTED.
GES IN PARENTHESES APPLY
TO MODEL LCS-B-6. A
READING APPLIES TO BOTH
S.

7. COAT BOTH SIDES OF INSULATING WAFER WITH DOW CORNING NO 340 SILICONE GREASE.

8. CR22 NOT USED ON UNITS WITH SERIAL NO PREFIX C.

THIS SCHEMATIC APPLIES TO UNITS BEARING SERIAL NO PREFIXES C AND D.

EL5VL064

Figure FO-7(1). −5 V DC Power Supply PS1, Schematic Diagram (Sheet 1 of 2).

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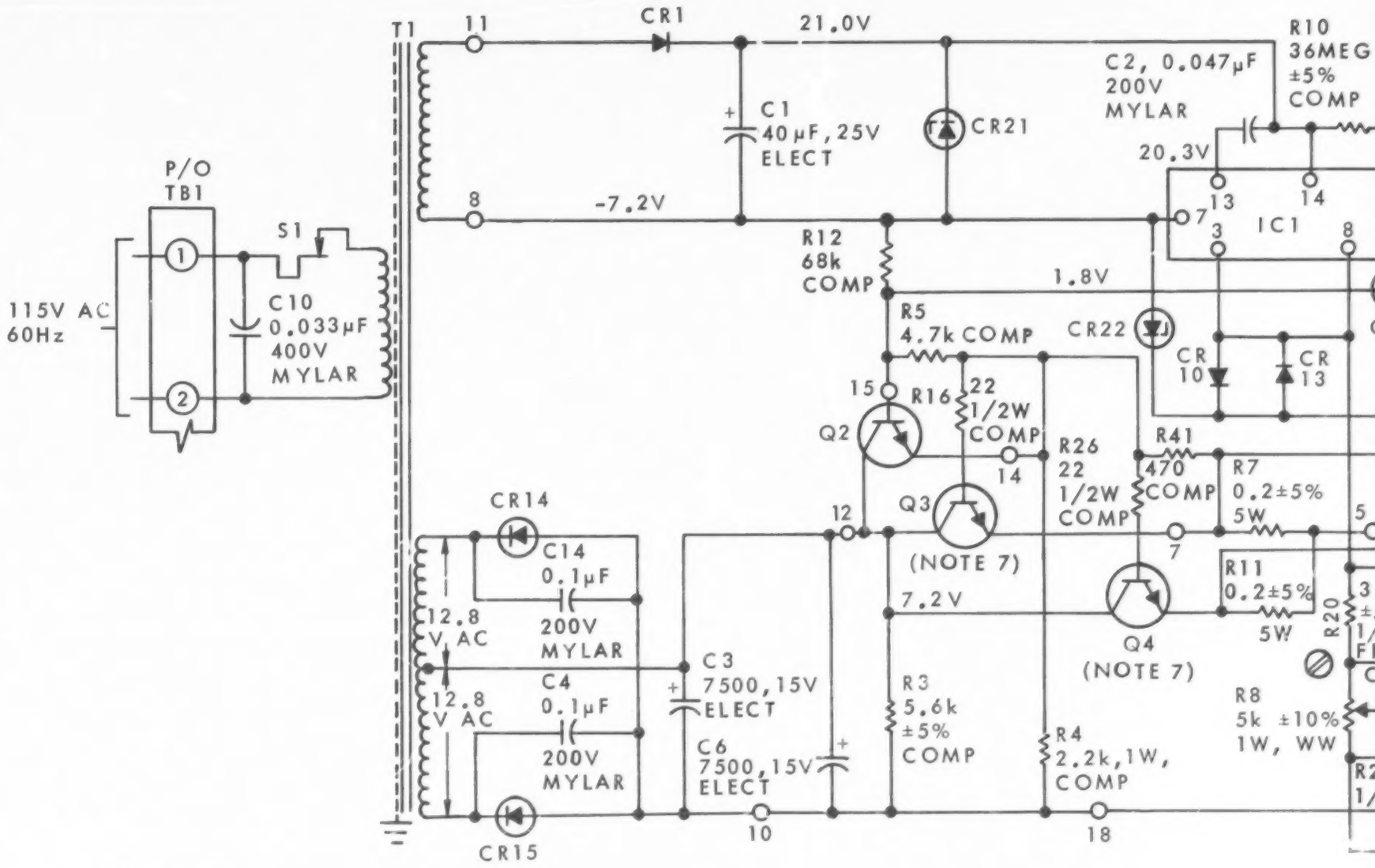
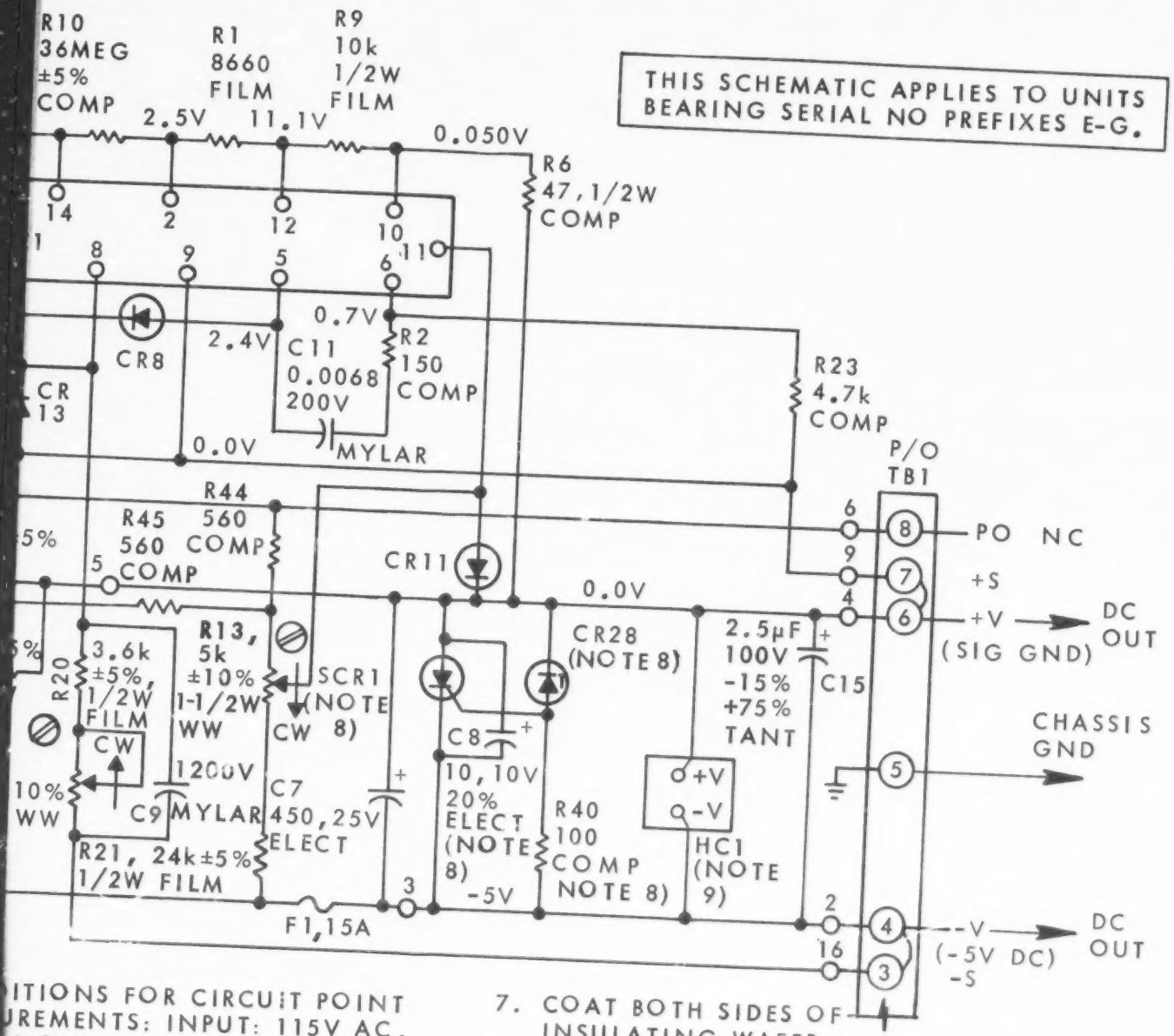


NOTES:

1. RESISTOR VALUES ARE IN OHMS.
2. RESISTOR WATTAGE 1/4 WATT: RESISTORS ABOVE 2 WATTS ARE WIREWOUND UNLESS OTHERWISE NOTED.
3. RESISTOR TOLERANCES: COMP. ±10%; WIREWOUND ±2%; FILM ±1%; UNLESS OTHERWISE NOTED.
4. CAPACITOR TOLERANCES: ELECTROLYTIC -10%,+100%: MYLAR ±10%; CERAMIC 10%; UNLESS OTHERWISE NOTED.
5. SYMBOLS:
   - ⏚ INDICATES CONNECTION TO CHASSIS.
   - ⊘ INDICATES ADJUSTMENT OF CALIBRATION CONTROL.
   - —○— INDICATES TERMINAL ON PRINTED WIRING BOARD.
6. CONDITION
   MEASUREMEN
   60Hz; NOM.
   LOAD. INDI
   TYPICAL VA
   DC UNLESS
   DC MEASURE
   20,000 OHM
   BETWEEN +S
   POINTS UNL
   SHORTED, -



ITIONS FOR CIRCUIT POINT
UREMENTS: INPUT: 115V AC,
NOM. RATED VOLTAGE NO
INDICATED VOLTAGES ARE
AL VALUES AND ARE
LESS OTHERWISE NOTED.
ASUREMENTS TAKEN WITH
OHMS/V VOLTMETER
EN +S(TERM 7) AND INDICATED
S UNLESS NOTED; +S AND +V
ED, -S AND -V SHORTED.

7. COAT BOTH SIDES OF INSULATING WAFER WITH DOW CORNING NO 340 SILICONE GREASE.
8. C8, CR28, R40 AND SCR1 ONLY USED ON MODEL LCS-B-5-OV WITH SERIAL NO PREFIX E.
9. HC1 ONLY USED ON MODEL LCS-B-5-OV WITH SERIAL NO PREFIXES FROM F ON.

EL5VL074

Figure FO-7(2). −5 V DC Power Supply PS1, Schematic Diagram (Sheet 2 of 2).

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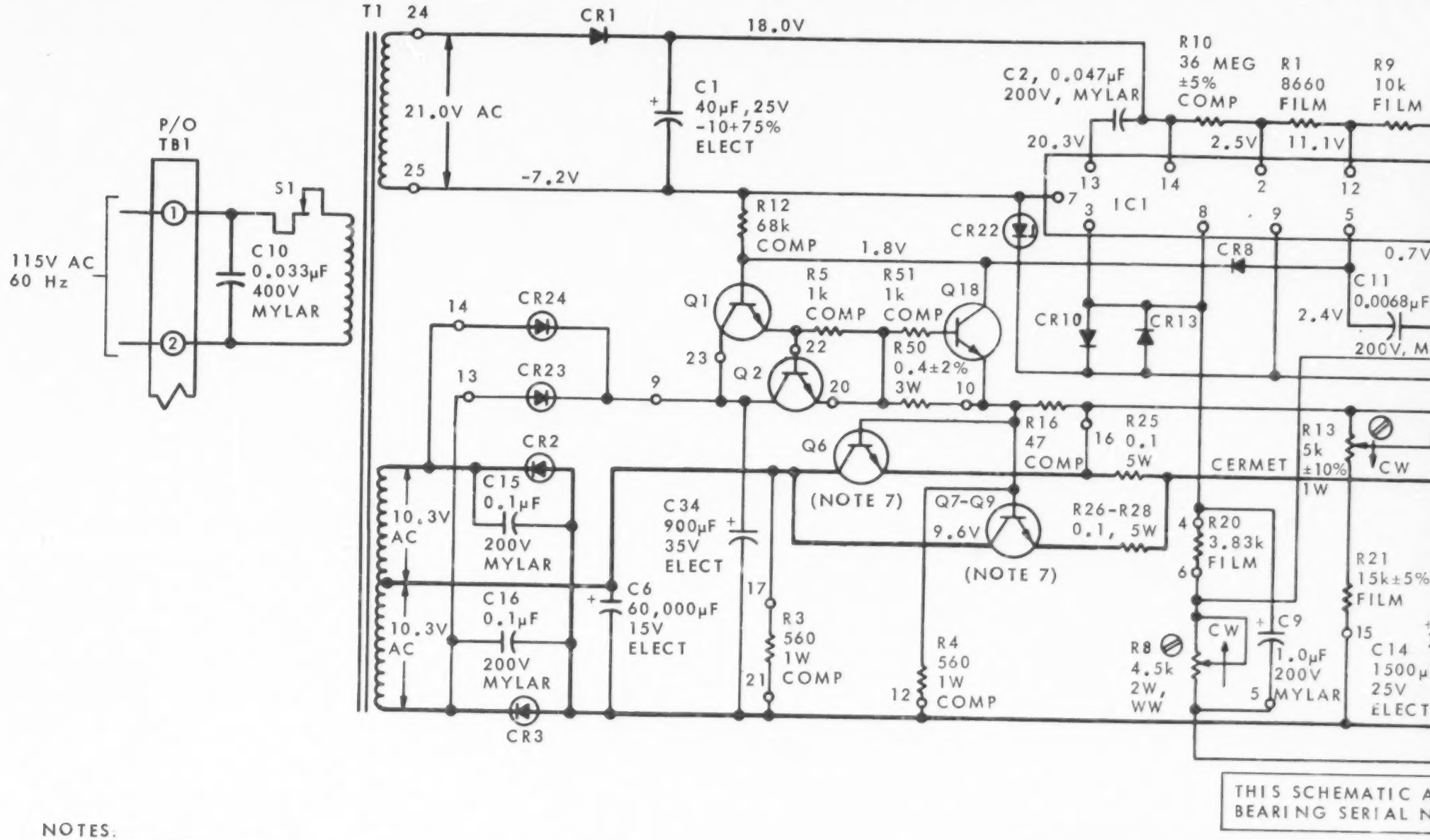
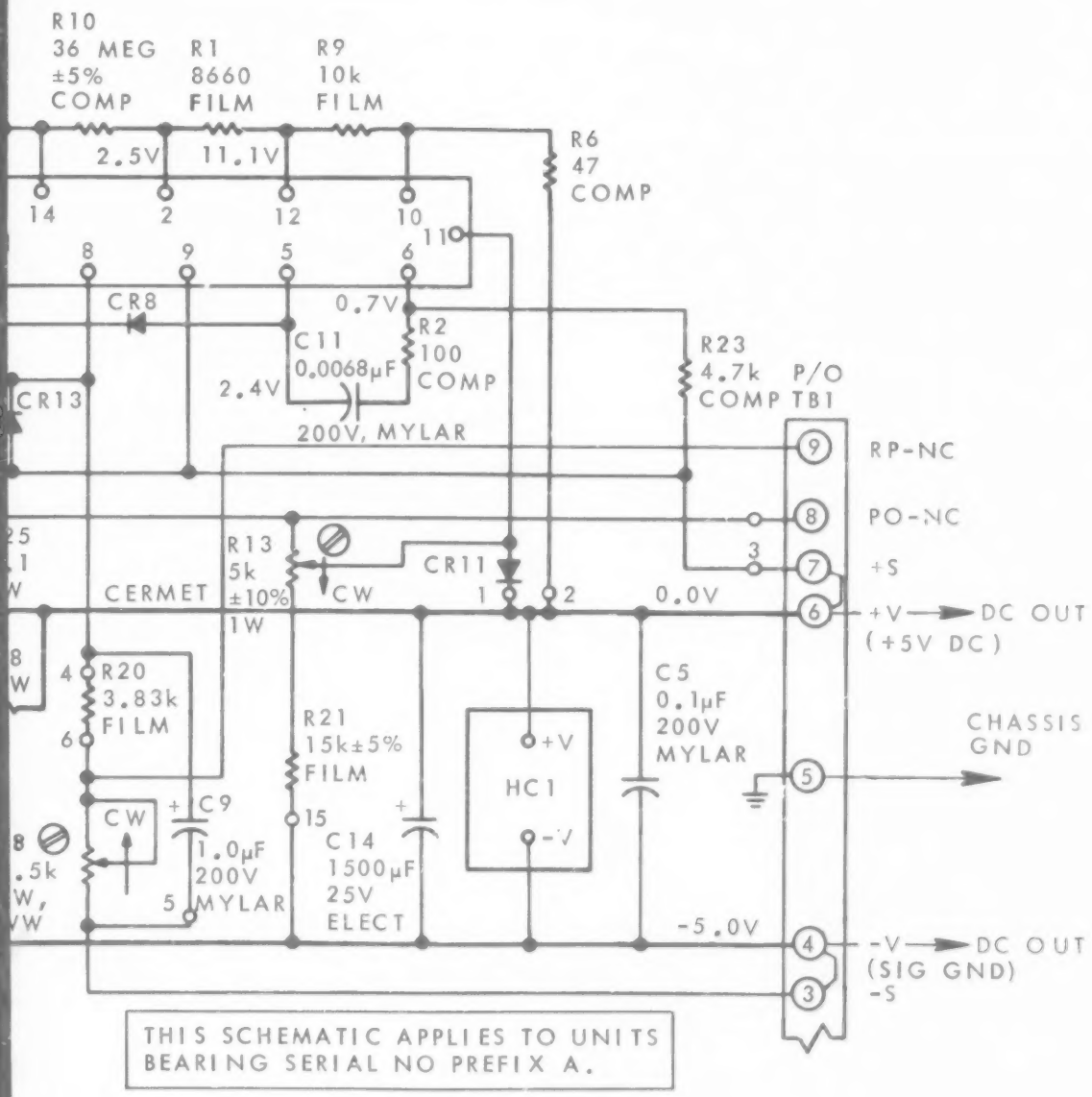


THIS SCHEMATIC A
BEARING SERIAL N

NOTES.

1. RESISTOR VALUES ARE IN OHMS.
2. RESISTOR WATTAGE 1/4 WATT; RESISTORS ABOVE 2 WATTS ARE WIREWOUND UNLESS OTHERWISE NOTED.
3. RESISTOR TOLERANCES: COMP ±10%; WIREWOUND ±5%; FILM ±1%; UNLESS OTHERWISE NOTED.
4. CAPACITOR TOLERANCES: ELECTROLYTIC -10%,+100%; MYLAR ±10%; CERAMIC 10%; UNLESS OTHERWISE NOTED.
5. SYMBOLS:
   - ⏚ INDICATES CONNECTION TO CHASSIS.
   - ⊘ INDICATES ADJUSTMENT OF CALIBRATION CONTROL
   - ⊸ INDICATES TERMINAL ON PRINTED WIRING BOARD.
6. CONDITIONS FOR CIRCUIT POINT MEASUREMENTS: INPUT: 115V AC, 60Hz; NOM RATED VOLTAGE NO LOAD. INDICATED VOLTAGES ARE TYPICAL VALUES AND ARE DC UNLESS OTHERWISE NOTED. DC MEASUREMENTS TAKEN WITH 20,000 OHMS/V VOLTMETER BETWEEN +S(TERM 7) AND INDICATED POINTS UNLESS NOTED; +S AND +V SHORTED, -S AND -V SHORTED.

Figure FO-8. +5 V DC Power S



THIS SCHEMATIC APPLIES TO UNITS BEARING SERIAL NO PREFIX A.

FOR CIRCUIT POINT
TS: INPUT: 115V AC,
ATED VOLTAGE NO
ATED VOLTAGES ARE
UES AND ARE DC UNLESS
NOTED. DC MEASUREMENTS
20,000 OHMS/V VOLTMETER
ERM 7) AND INDICATED
SS NOTED; +S AND +V
AND -V SHORTED.

7. COAT BOTH SIDES OF INSULATING WAFER WITH DOW CORNING NO 340 SILICONE GREASE.

EL5VL062

Figure FO-8. +5 V DC Power Supply PS2, Schematic Diagram

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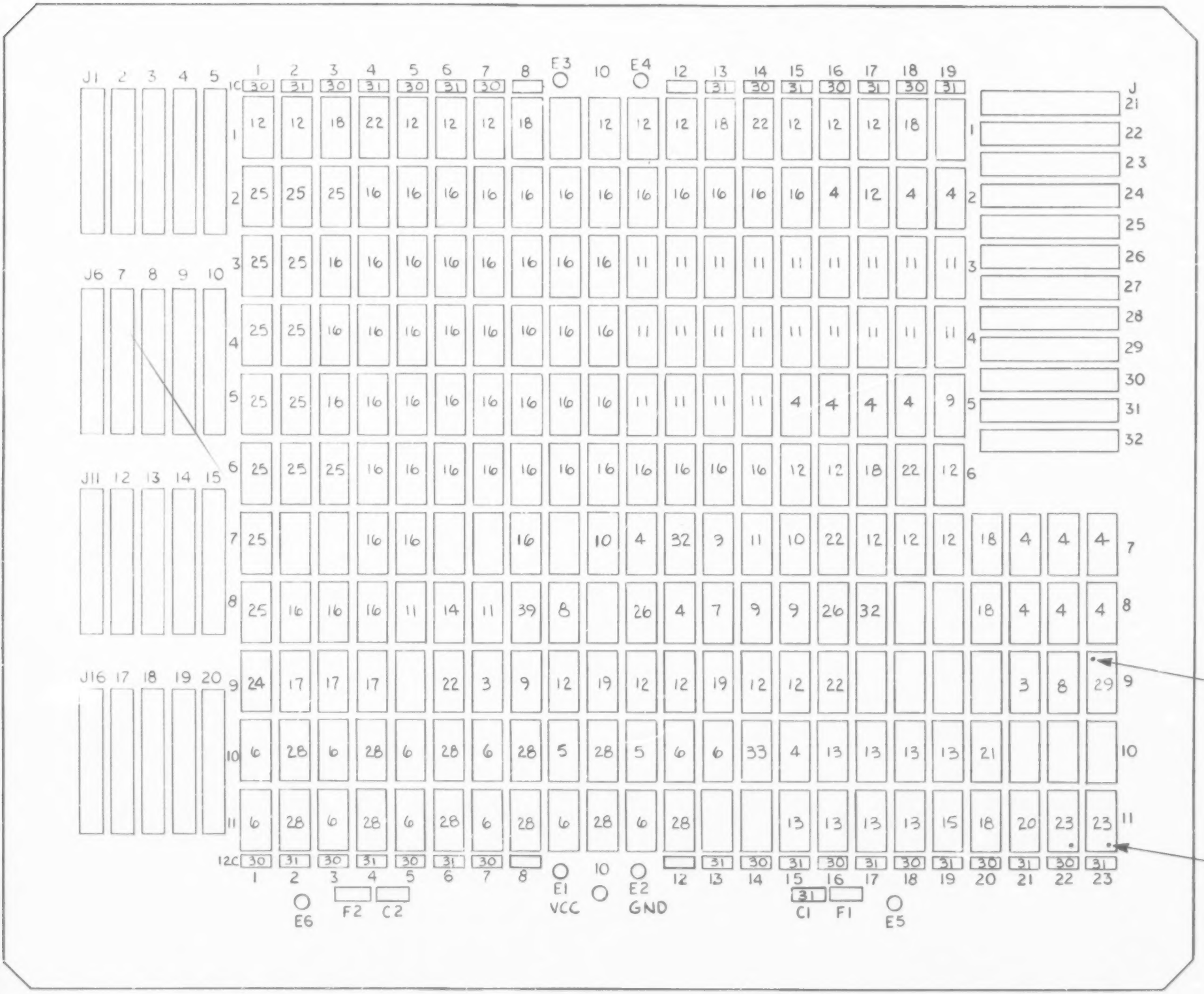

ITEM NO	MODULE TYPE	GENERIC IC NO
3	2GK-1	74LS00
4	1GK-1	74SL04
5	1GO-2	7406
6	1QO-1	7407
7	3GK-1	74LS10
8	2IK-1	74LS32
9	2GDK-1	74LS37
10	2QNK-1	74LS51
11	DFA-1	7474
12	MVC-1	74123
13	4BCBK-1	74LS161
14	MVDK-1	74LS221
15	OSAK-1	74LS124
16	LRA	75107
17	LDA	75110
18	CAP102	926CX7R102M050
19	CAP104	926CX7R104M050
20	CAP332	926CX7R332M050
21	REV102	916C1J2X2PD
22	REV223	916C223X2PE
23	REA103	3099P-1-103
24	TER1	398-14942-4
25	TER2	398-14942-3
26	9PGBK-1	74LS280
28	REV151	916C151X2PE
29	3GK	74LS11
30	N/A	7CZ5U225X0050E4
31	N/A	7CZ5U104X0050D1
32	RES102	899-3-91K
33	3NK	74LS27
39	RC	398-15858-1

EL5VL080

Figure FO-9. SSCC Logic Board A4, Parts Location Diagram.

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